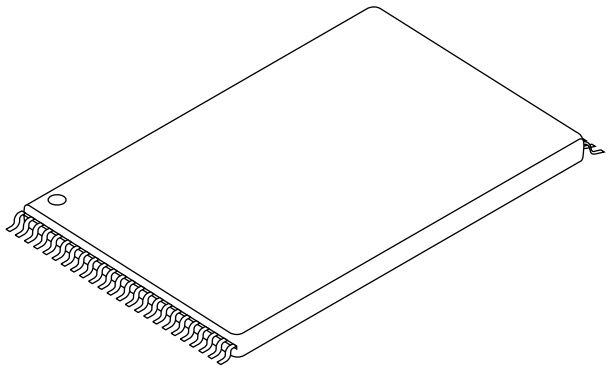
NAND Flash Memory

MT29F2G08AABWP/MT29F2G16AABWP
MT29F4G08BABWP/MT29F4G16BABWP
MT29F8G08FABWP

Features

- Organization:
  - Page size:
    x8: 2,112 bytes (2,048 + 64 bytes)
    x16: 1,056 words (1,024 + 32 words)
  - Block size: 64 pages (128K + 4K bytes)
  - Device size: 2Gb: 2,048 blocks; 4Gb: 4,096 blocks; 8Gb: 8,192 blocks
- Read performance:
  - Random read: 25µs
  - Sequential read: 30ns (3V x8 only)
- Write performance:
  - Page program: 300µs (TYP)
  - Block erase: 2ms (TYP)
- Endurance: 100,000 PROGRAM/ERASE cycles
- Data retention: 10 years
- First block (block address 00h) guaranteed to be valid without ECC (up to 1,000 PROGRAM/ERASE cycles)
- VCC: 2.7V–3.6V
- Automated PROGRAM and ERASE
- Basic NAND command set:
  - PAGE READ, RANDOM DATA READ, READ ID, READ STATUS, PROGRAM PAGE, RANDOM DATA INPUT, PROGRAM PAGE CACHE MODE, INTERNAL DATA MOVE, INTERNAL DATA MOVE with RANDOM DATA INPUT, BLOCK ERASE, RESET
- New commands:
  - PAGE READ CACHE MODE
  - READ UNIQUE ID (contact factory)
  - READ ID2 (contact factory)
- Operation status byte provides a software method of detecting:
  - PROGRAM/ERASE operation completion
  - PROGRAM/ERASE pass/fail condition
  - Write-protect status
- Ready/busy# (R/B#) pin provides a hardware method of detecting PROGRAM or ERASE cycle completion
- PRE pin: prefetch on power up
- WP# pin: hardware write protect

Figure 1: 48-Pin TSOP Type 1



Options	Marking
• Density:	
2Gb (single die)	MT29F2GxxAAB
4Gb (dual-die stack)	MT29F4GxxBAB
8Gb (quad-die stack)	MT29F8GxxFAB
• Device width:	
x8	MT29Fxx08x
x16	MT29Fxx16x

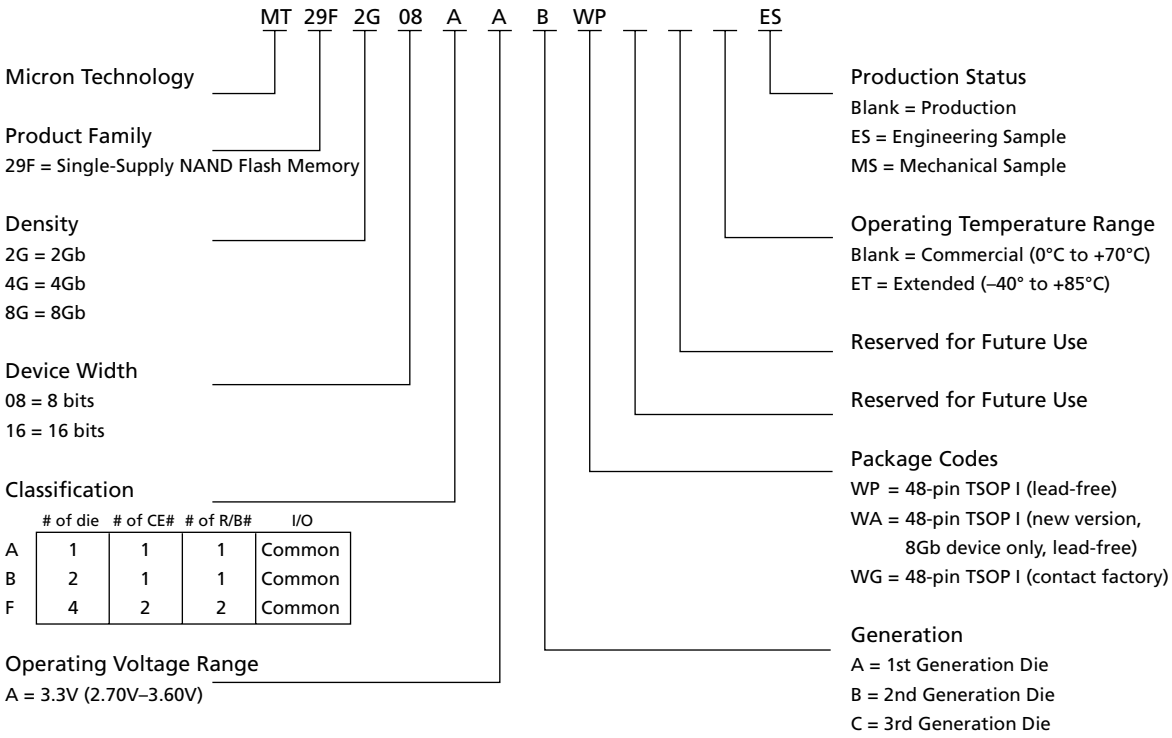
• Configuration:	# of die	# of CE#	# of R/B#	
	1	1	1	A
	2	1	1	B
	4	2	2	F

• VCC: 2.7V–3.6V	A
• Second generation die	B
• Package:	
48 TSOP type I (lead-free)	WP
48 TSOP type I (NEW version, 8Gb device only, lead-free)	WA
48 TSOP type I (contact factory)	WG
• Operating temperature:	
Commercial (0°C to 70°C)	None
Extended temperature (-40°C to +85°C)	ET

Part Numbering Information

Micron® NAND Flash devices are available in several different configurations and densities. (See Figure 2.)

Figure 2: Part Number Chart



Valid Part Number Combinations

After building the part number from the part numbering chart above, verify that the part number is valid using the Micron Parametric Part Search Web site at http://www.micron.com/partsearch to verify that the part number is offered and valid. If the device required is not on this list, contact the factory.

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General Description

NAND technology provides a cost-effective solution for applications requiring high-density solid-state storage. The MT29F2G08AxB and MT29F2G16AxB are 2Gb NAND Flash memory devices. The MT29F4G08BxB and MT29F4G16BxB are two-die stacks that operate as a single 4Gb device. The MT29F8G08FAB is a four-die stack that operates as two independent 4Gb devices (MT29F4G08BxB), providing a total storage capacity of 8Gb in a single, space-saving package. Micron NAND Flash devices include standard NAND features as well as new features designed to enhance system-level performance.

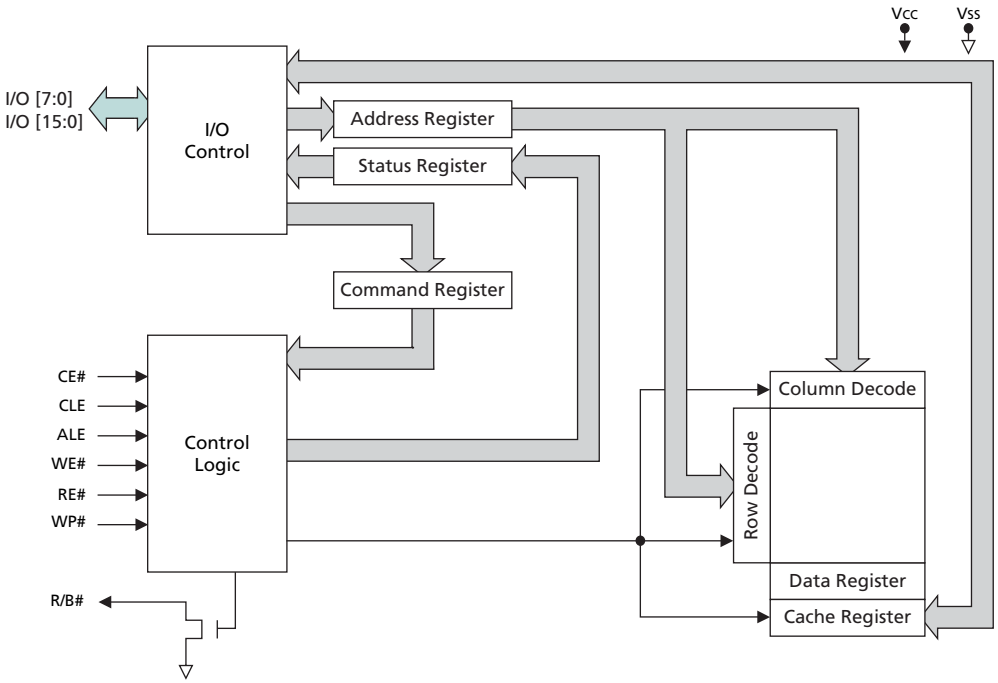
Micron NAND Flash devices use a highly multiplexed 8- or 16-bit bus (I/O[7:0] or I/O[15:0]) to transfer data, addresses, and instructions. The five command pins (CLE, ALE, CE#, RE#, WE#) implement the NAND command bus interface protocol. Three additional pins control hardware write protection (WP#), monitor device status (R/B#), and initiate the auto-read feature (PRE—3V device only). Note that the PRE function is not supported on extended-temperature devices.

This hardware interface creates a low-pin-count device with a standard pinout that is the same from one density to another, allowing future upgrades to higher densities without board redesign.

MT29F2G and MT29F4G devices contain 2,048 and 4,096 erasable blocks respectively. Each block is subdivided into 64 programmable pages. Each page consists of 2,112 bytes (x8) or 1,056 words (x16). The pages are further divided into a 2,048-byte data storage region with a separate 64-byte area on the x8 device; and on the x16 device, separate 1,024-word and 32-word areas. The 64-byte and 32-word areas are typically used for error management functions.

The contents of each 2,112-byte page can be programmed in 300µs, and an entire 132K-byte/66K word block can be erased in 2ms. On-chip control logic automates PROGRAM and ERASE operations to maximize cycle endurance. ERASE/PROGRAM endurance is specified at 100,000 cycles when using appropriate error correcting code (ECC) and error management.

Figure 3: NAND Flash Functional Block Diagram



Note: The PRE function is not supported on extended-temperature devices.

Figure 4: Pin Assignment (Top View) 48-Pin TSOP Type 1

x16	x8			x8	x16
NC	NC	1 ●	48	NC	Vss
NC	NC	2	47	NC	I/O15
NC	NC	3	46	NC	I/O7
NC	NC	4	45	NC	I/O14
NC	NC	5	44	I/O7	I/O6
NC	R/B2#[1]	6	43	I/O6	I/O13
R/B#	R/B#	7	42	I/O5	I/O5
RE#	RE#	8	41	I/O4	I/O12
CE#	CE#	9	40	NC	I/O4
NC	CE2#[1]	10	39	NC	NC
NC	NC	11	38	PRE/Vss[2]	PRE/Vss[2]
Vcc	Vcc	12	37	Vcc	Vcc
Vss	Vss	13	36	Vss	NC
NC	NC	14	35	NC	NC
NC	NC	15	34	NC	NC
CLE	CLE	16	33	NC	I/O11
ALE	ALE	17	32	I/O3	I/O3
WE#	WE#	18	31	I/O2	I/O10
WP#	WP#	19	30	I/O1	I/O2
DNU	DNU	20	29	I/O0	I/O9
DNU	DNU	21	28	NC	I/O1
DNU	DNU	22	27	NC	I/O8
NC	NC	23	26	NC	I/O0
NC	NC	24	25	NC	Vss

Notes: 1. CE2# and R/B2# on 8Gb device only. These pins are NC for other configurations.
2. The PRE function is not supported on extended-temperature devices.

Table 1: Pin Descriptions

Symbol	Type	Description
ALE	Input	Address latch enable: During the time ALE is HIGH, address information is transferred from I/O[7:0] into the on-chip address register upon a LOW-to-HIGH transition on WE#. When address information is not being loaded, the ALE pin should be driven LOW.
CE#, CE2#	Input	Chip enable: Gates transfers between the host system and the NAND device. Once the device starts a PROGRAM or ERASE operation, the chip enable pin can be de-asserted. For the 8Gb configuration, CE# controls the first 4Gb of memory; CE2# controls the second 4Gb. See the Bus Operation section, starting on "Bus Operation" on page 16 for additional operational details.
CLE	Input	Command latch enable: When CLE is HIGH, information is transferred from I/O[7:0] to the on-chip command register on the rising edge of WE#. When command information is not being loaded, the CLE pin should be driven LOW.
PRE[1] (3V device only)	Input	Power-on read enable: Enables the auto-read function when at Vcc. See "Bus Operation" on page 16, for additional details.
RE#	Input	Read enable: Gates transfers from the NAND device to the host system.
WE#	Input	Write enable: Gates transfers from the host system to the NAND device.
WP#	Input	Write protect: Pin protects against inadvertent PROGRAM and ERASE operations. All PROGRAM and ERASE operations are disabled when the WP# pin is LOW.
I/O[7:0] MT29FxG08 I/O[15:0] MT29FxG16	I/O	Data inputs/outputs: The bidirectional I/O pins transfer address, data, and instruction information. Data is output only during READ operations; at other times the I/O pins are inputs.
R/B#, R/B2#	Output	Ready/busy: An *open-drain,* active-LOW output, that uses an external pull-up resistor. The pin is used to indicate when the chip is processing a PROGRAM or ERASE operation. The pin is also used during a READ operation to indicate when data is being transferred from the array into the serial data register. Once these operations have completed, the R/B# returns to the High-Z state. In the 8Gb configuration, R/B# is for the 4Gb of memory enabled by CE#; R/B2# is for the 4Gb of memory enabled by CE2#.
Vcc	Supply	Vcc: The Vcc pin is the power supply pin.
Vss	Supply	Vss: The Vss pin is the ground connection.
DNU	–	Do not use: Must be left floating.
NC	–	No connect: NC pins are not internally connected. These pins can be driven or left unconnected.

Notes: 1. The PRE function is not supported on extended-temperature devices.

Architecture

These devices use NAND electrical and command interfaces. Data, commands, and addresses are multiplexed onto the same pins. This provides a memory device with a low pin count.

The internal memory array is accessed on a page basis. When doing reads, a page of data is copied from the memory array into the data register. Once copied to the data register, data is output sequentially, byte-by-byte on x8 devices, or word-by-word on x16 devices.

The memory array is programmed on a page basis. After the starting address is loaded into the internal address register, data is sequentially written to the internal data register up to the end of a page. After all of the page data has been loaded into the data register, array programming is started.

In order to increase programming bandwidth, this device incorporates a cache register. In the cache programming mode, data is first copied into the cache register and then into the data register. Once the data is copied into the data register, programming begins.

After the data register has been loaded and programming started, the cache register becomes available for loading additional data. Loading the next page of data into the cache register takes place while page programming is in process.

The INTERNAL DATA MOVE command also uses the internal cache register. Normally, moving data from one area of external memory to another uses a large number of external memory cycles. By using the internal cache register and data register, array data can be copied from one page and then programmed into another without using external memory cycles.

Addressing

NAND Flash devices do not contain dedicated address pins. Addresses are loaded using a five-cycle sequence as shown in Figures 7 and 8, on pages 12 and 13 respectively. Table 2 on page 12 presents address functions internal to the x8 device; Table 3 on page 13 covers the same functions for the x16 device. See Figures 5 and 6 on page 11 for additional memory mapping and addressing details.

Figure 5: Memory Map x8

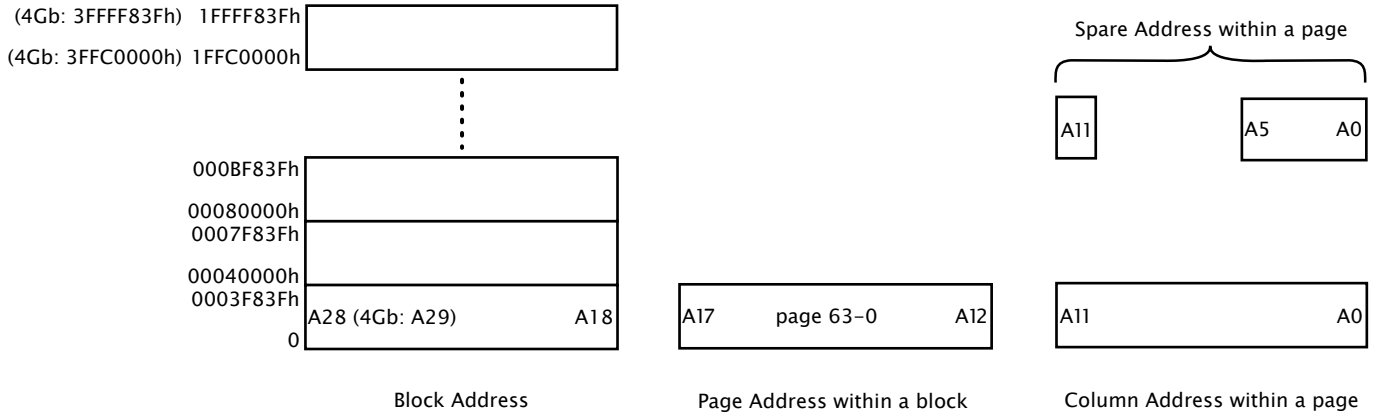
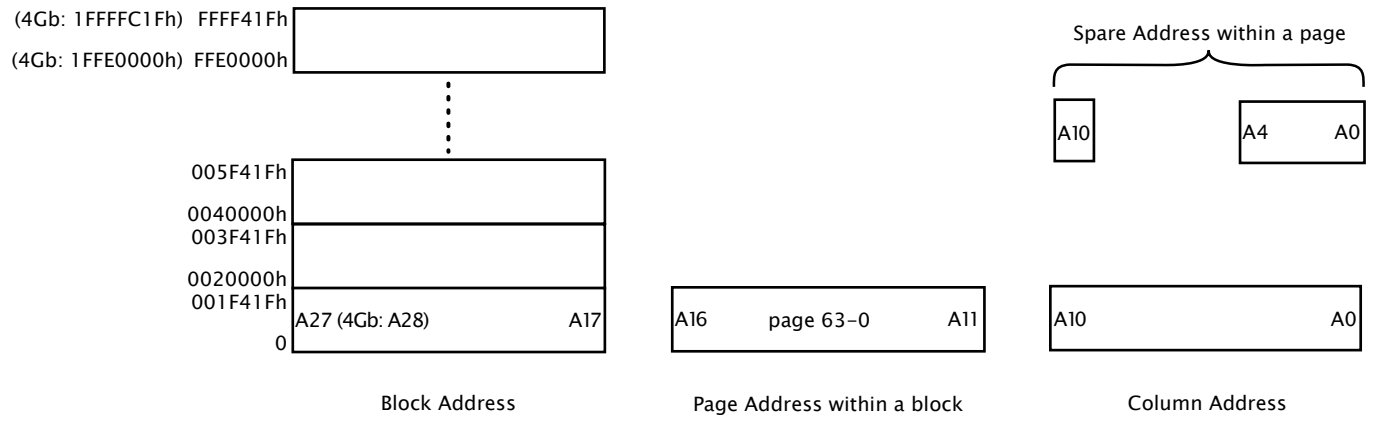


Figure 6: Memory Map x16



Note: Block address and page address = actual page address.

Figure 7: Array Organization for MT29F2G08AxB (x8)

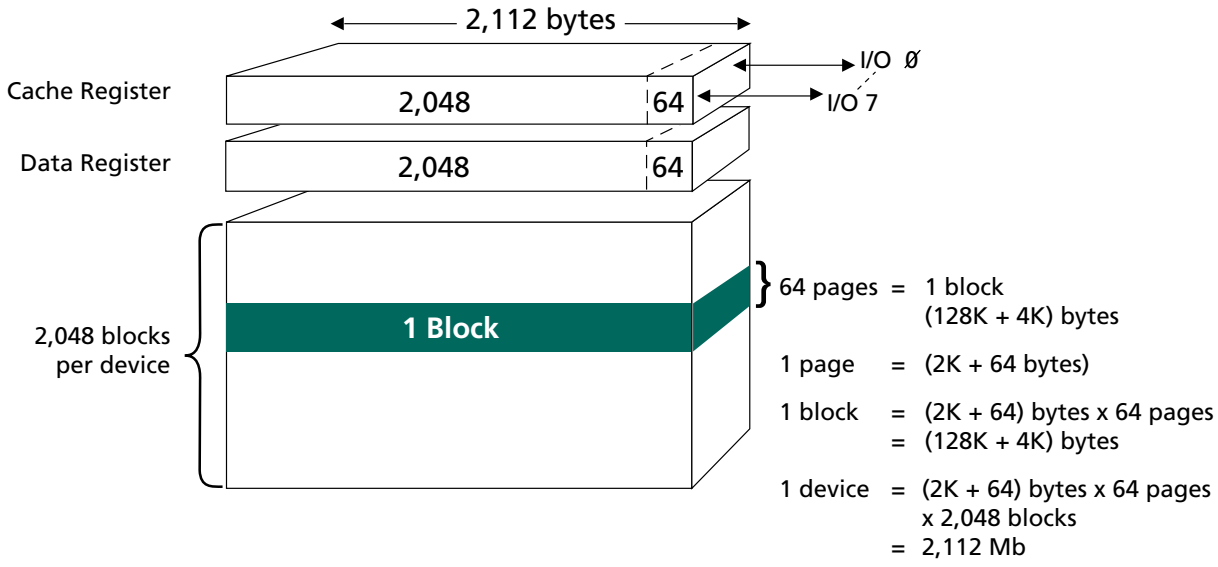


Table 2: Array Addressing: MT29F2G08AxB

Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	LOW	CA11	CA10	CA9	CA8
Third	RA19	RA18	RA17	RA16	RA15	RA14	RA13	RA12
Fourth	RA27	RA26	RA25	RA24	RA23	RA22	RA21	RA20
Fifth	LOW	LOW	LOW	LOW	LOW	LOW	LOW	RA28

Note: CAx = column address; RAx = row address.

Figure 8: Array Organization for MT29F2G16AxB (x16)

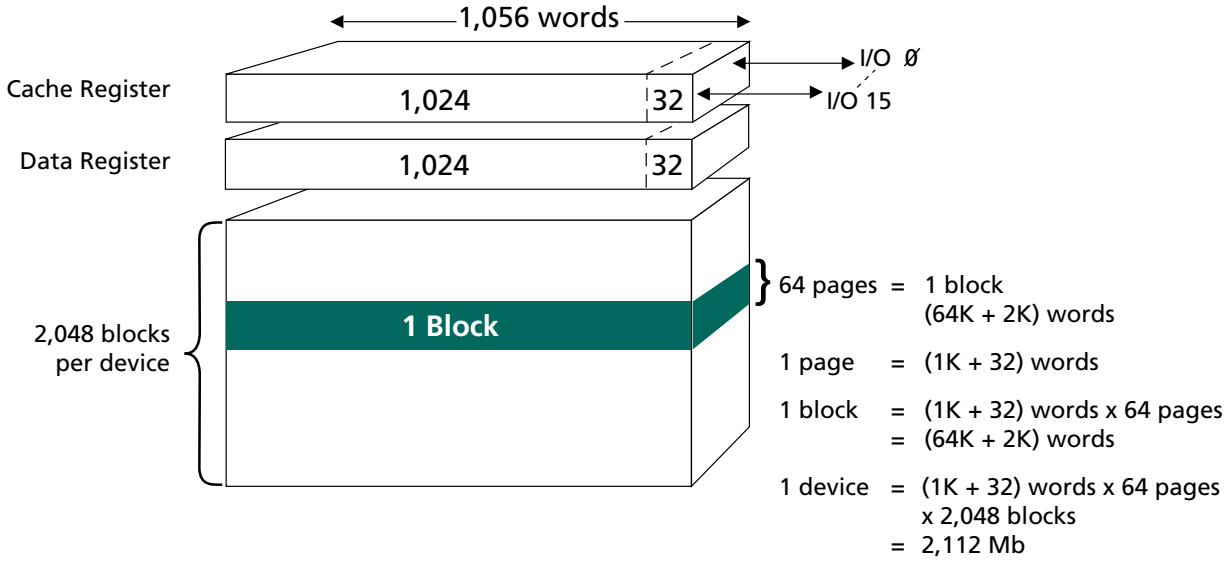
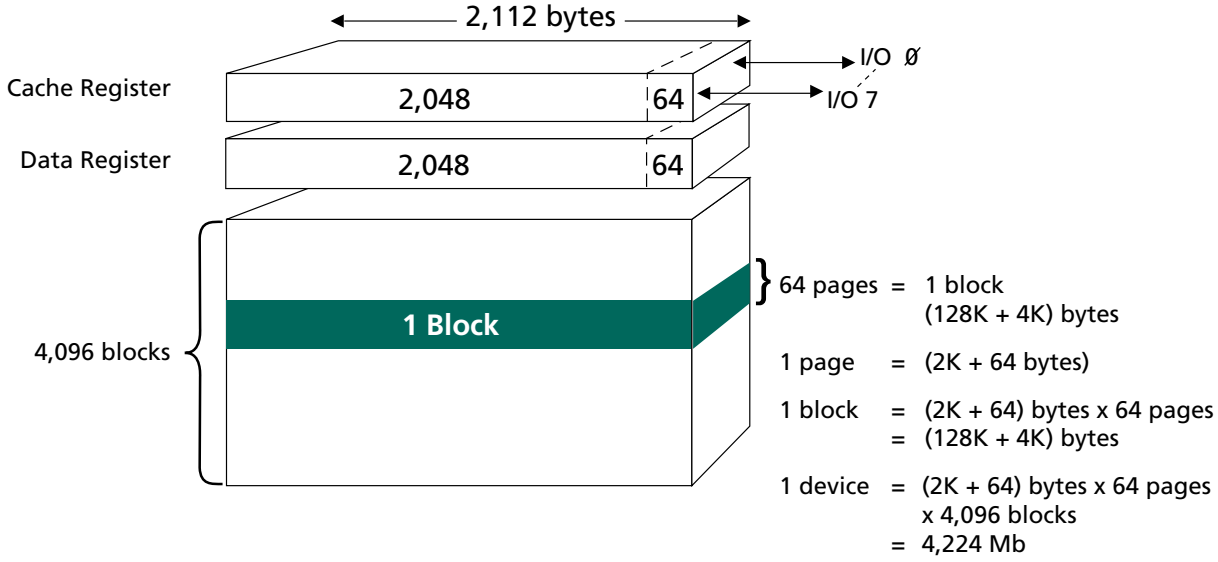


Table 3: Array Addressing: MT29F2G16AxB

Cycle	I/O[15:8]	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	LOW	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	LOW	LOW	LOW	CA10	CA9	CA8
Third	LOW	RA18	RA17	RA16	RA15	RA14	RA13	RA12	RA11
Fourth	LOW	RA26	RA25	RA24	RA23	RA22	RA21	RA20	RA19
Fifth	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	RA27

Notes: 1. CAx = column address; RAx = row address.
2. I/O[15:8] are not used during the addressing sequence and should be driven LOW.

Figure 9: Array Organization for MT29F4G08BxB and MT29F8G08FxB (x8)



Note: For the 8Gb MT29F8G08F, the 4Gb array organization shown here applies to each chip enable (CE# and CE2#).

Table 4: Array Addressing: MT29F4G08BxB and MT29F8G08FxB

CAx = column address; RAx = row address.

Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	LOW	CA11	CA10	CA9	CA8
Third	RA19	RA18	RA17	RA16	RA15	RA14	RA13	RA12
Fourth	RA27	RA26	RA25	RA24	RA23	RA22	RA21	RA20
Fifth	LOW	LOW	LOW	LOW	LOW	LOW	RA29[1]	RA28

Notes: 1. Die address boundary: 0 = 0 – 2Gb, 1 = 2Gb – 4Gb.

Figure 10: Array Organization for MT29F4G16BxB (x16)

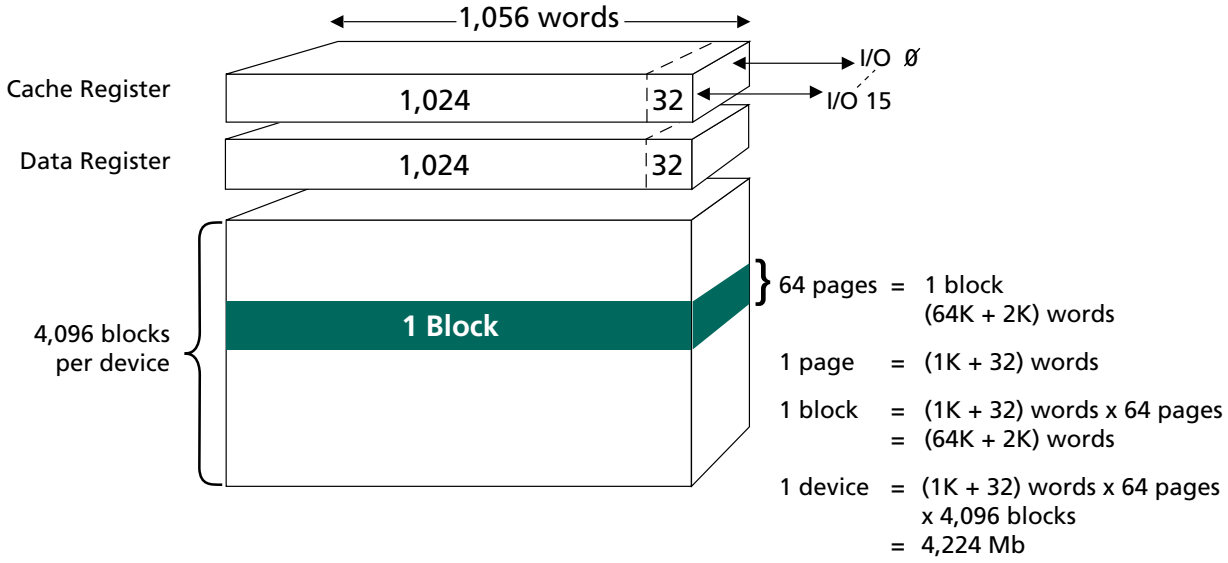


Table 5: Array Addressing: MT29F4G16BxB

CAx = column address; RAx = row address.

Cycle	I/O[15:8]	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	LOW	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	LOW	LOW	LOW	CA10	CA9	CA8
Third	LOW	RA18	RA17	RA16	RA15	RA14	RA13	RA12	RA11
Fourth	LOW	RA26	RA25	RA24	RA23	RA22	RA21	RA20	RA19
Fifth	LOW	LOW	LOW	LOW	LOW	LOW	LOW	RA28[1]	RA27

Notes: 1. Die address boundary: 0 = 0 – 2Gb, 1 = 2Gb – 4Gb.
2. I/O[15:8] are not used during the addressing sequence and should be driven LOW.

Bus Operation

The bus on the MT29Fxxx devices is multiplexed. Data I/O, addresses, and commands all share the same pins. I/O pins I/O[15:8] are used only for data in the x16 configuration. Addresses and commands are always supplied on I/O[7:0].

The command sequence normally consists of a command latch cycle, an ADDRESS LATCH cycle, and a DATA cycle—either READ or WRITE.

Control Signals

CE#, WE#, RE#, CLE, ALE and WP# control Flash device READ and WRITE operations. On the 8Gb MT29F8G08FAB, CE# and CE2# each control independent 4Gb arrays. CE2# functions the same as CE# for its own array; all operations described for CE# also apply to CE2#.

CE# is used to enable the device. When CE# is LOW and the device is not in the busy state, the Flash memory will accept command, data, and address information.

When the device is not performing an operation, the CE# pin is typically driven HIGH and the device enters standby mode. The memory will enter standby if CE# goes HIGH while data is being transferred and the device is not busy. This helps reduce power consumption. See Figure 40 on page 45 and Figure 47 on page 50 for examples of CE# "Don't Care" operations.

The CE# "Don't Care" operation allows the NAND Flash to reside on the same asynchronous memory bus as other Flash or SRAM devices. Other devices on the memory bus can then be accessed while the NAND Flash is busy with internal operations. This capability is important for designs that require multiple NAND Flash devices on the same bus. One device can be programmed while another is being read.

A HIGH CLE signal indicates that a command cycle is taking place. A HIGH ALE signal signifies that an address input cycle is occurring.

Commands

Commands are written to the command register on the rising edge of WE# when:

- CE# and ALE are LOW, and
- CLE is HIGH, and
- The device is not busy

The exceptions to this are the READ STATUS and RESET commands. Commands are transferred to the command register on the rising edge of WE#. See Figure 34 on page 42.

Commands are input on I/O[7:0] only. For devices with a x16 interface, I/O[15:8] must be written with zeros when issuing a command.

Address Input

Addresses are written to the address register on the rising edge of WE# when:

- CE# and CLE are LOW, and
- ALE is HIGH, and
- The device is not busy

Addresses are input on I/O[7:0] only. For devices with a x16 interface, I/O[15:8] must be written with zeros when issuing an address.

Generally all five ADDRESS cycles are written to the device. An exception to this is the BLOCK ERASE command, which requires only three ADDRESS cycles. See "BLOCK ERASE Operation" on page 33 for details.

RANDOM DATA INPUT and OUTPUT commands need only column addresses, so only two ADDRESS cycles are required. Refer to the command descriptions to determine the addressing requirements for each command.

Data Input

Data is written to the data register on the rising edge of WE# when:

- CE#, CLE, and ALE are LOW, and
- The device is not busy

Data is input on I/O[7:0] for x8 devices, and I/O[15:0] on x16 devices. See Figure 36 on page 43 for additional data input details.

READs

After a READ command is sent to the memory device, data is transferred from the memory array to the data register in ^{t}R. Typically ^{t}R is 25µs. When data is available in the data register, it is clocked out of the part by RE# going LOW. See Figure 39 on page 44 for detailed timing information.

The READ STATUS (70h) command or the R/B# signal can be used to determine when the device is ready. See the STATUS READ command section on page 27 for details.

Ready/Busy#

The R/B# output provides a hardware method of indicating the completion of a PROGRAM/ERASE/READ operation. The signal is typically HIGH, and transitions to LOW after the appropriate command is written to the device. The signal pin's open-drain driver enables multiple R/B# outputs to be OR-tied. The signal requires a pull-up resistor for proper operation. The READ STATUS command can be used in place of R/B#. Typically R/B# would be connected to an interrupt pin on the system controller. See Figure 12 on page 18.

On the 8Gb MT29F8G08FAB, R/B# provides an indication for the 4Gb section enabled by CE#, and R/B2# does the same for the 4Gb section enabled by CE2#. R/B# and R/B2# can be tied together, or they can be used separately to provide independent indications for each 4Gb section.

The combination of Rp and capacitive loading of the R/B# circuit determines the rise time of the R/B# pin. The actual value used for Rp (Rp = resistance of pull-up resistor) depends on the system timing requirements. Large values of Rp cause R/B# to be delayed significantly. At the 10- to 90-percent points on the R/B# waveform, rise time is approximately two time constants (TC).

Figure 11: Time Constants

$$TC = R \times C$$

Where R = Rp (resistance of pull-up resistor), and C = total capacitive load.

The fall time of the R/B# signal is determined mainly by the output impedance of the R/B# pin and the total load capacitance.

Refer to Figure 13 on page 18, and Figure 14 on page 19, which depict approximate Rp values using a circuit load of 100pF.

The minimum value for Rp is determined by the output drive capability of the R/B# signal, the output voltage swing, and V_{CC}.

Minimum Rp

$$Rp\ (MIN, 3.3V\ part) = \frac{V_{CC}\ (MAX) - V_{OL}\ (MAX)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

Where ΣIL is the sum of the input currents of all devices tied to the R/B# pin.

Figure 12: READY/BUSY# Open Drain

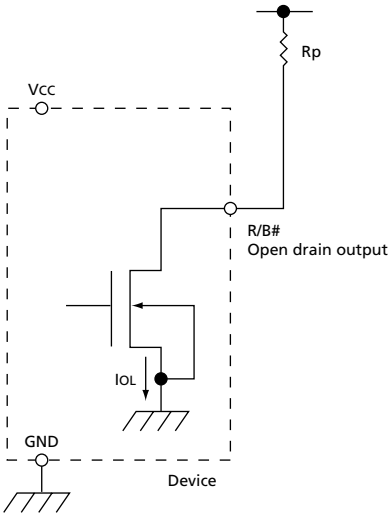
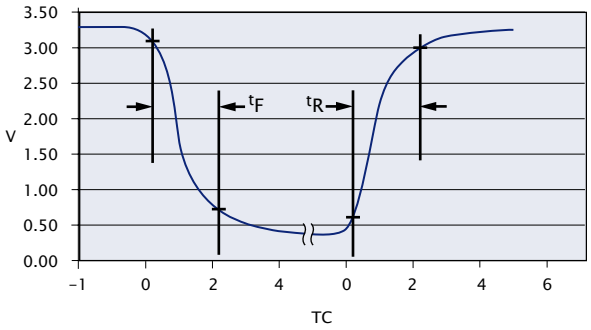


Figure 13: ^{t}R and ^{t}F



Notes:
1. ^{t}R and ^{t}F calculated at 10 percent and 90 percent points.
2. ^{t}R dependent on external capacitance and resistive loading and output transistor impedance.
3. ^{t}R primarily dependent on external pull-up resistor and external capacitive loading.
4. $^{t}F \approx 10ns$ at 3.3V.
5. See TC values in Figure 15 on page 19 for approximate Rp value and TC.

Figure 14: IOL vs. Rp

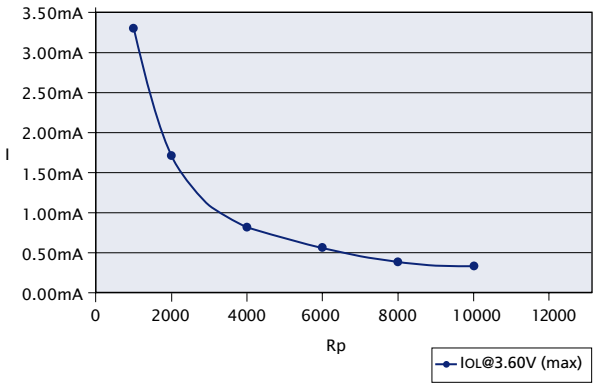


Figure 15: TC vs. Rp

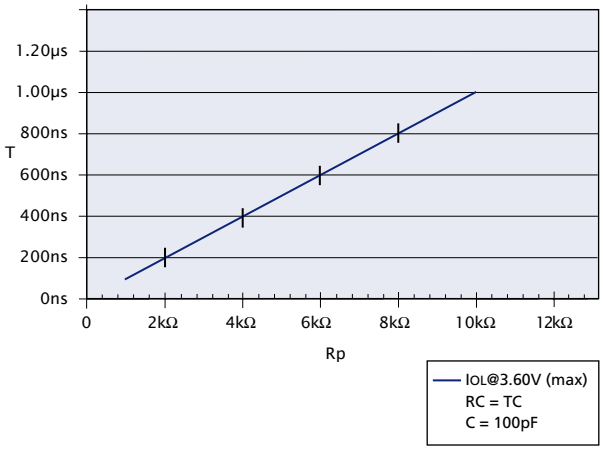


Table 6: Mode Selection

CLE	ALE	CE#	WE#	RE#	WP#[1]	PRE[2]	Mode	
H	L	L	↑	H	X	X	Read mode	Command input
L	H	L	↑	H	X	X		Address input
H	L	L	↑	H	H	X	Write mode	Command input
L	H	L	↑	H	H	X		Address input
L	L	L	↑	H	H	X	Data input	
L	L	L	H	↓	X	X	Sequential read and data output	
L	L	L	H	H	X	X	During read (busy)	
X	X	X	X	X	H	X	During program (busy)	
X	X	X	X	X	H	X	During erase (busy)	
X	X	X	X	X	L	X	Write protect	
X	X	H	X	X	0V/VCC	0V/VCC	Standby	

Notes: 1. WP# should be biased to CMOS HIGH or LOW for standby.
2. PRE should be tied to VCC or ground. Do not transition PRE during device operations. The PRE function is not supported on extended-temperature devices.
3. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = VIH or VIL.

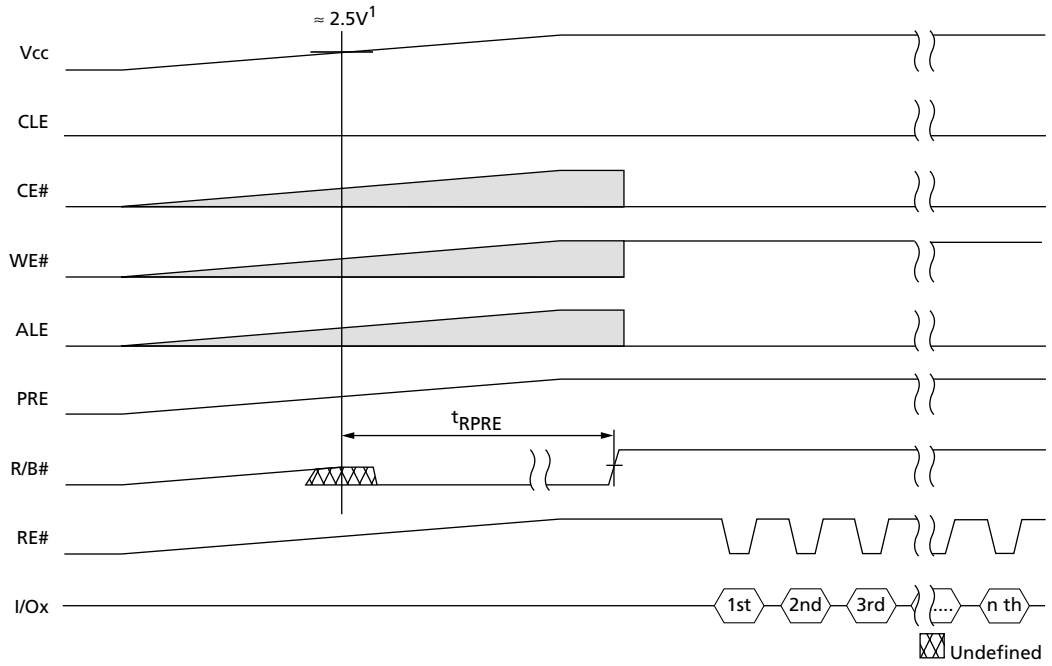
Power-On AUTO-READ

During power-on, with the PRE pin at VCC, 3V VCC devices automatically transfer the first page of the memory array to the data register without requiring a command or address-input sequence. As VCC reaches approximately 2.5V, the internal voltage detector initiates the power-on AUTO-READ function.

R/B# will stay LOW (^{t}RPRE) while the first page of data is copied into the data register. See Table 18 on page 41 for the ^{t}RPRE value. Once the READ is complete and R/B# goes HIGH, RE# can be pulsed to output the first page of data.

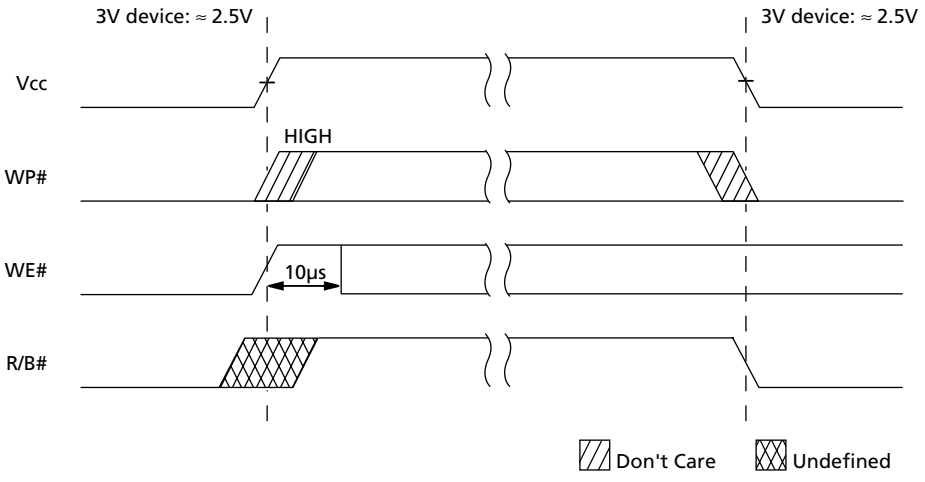
The PRE function is not supported on extended-temperature devices.

Figure 16: First Page Power-On AUTO-READ (3V Vcc only)



Notes: 1. Verified per device characterization; not 100 percent tested on all devices.
2. The PRE function is not supported on extended-temperature devices.

Figure 17: AC Waveforms During Power Transitions



Command Definitions

Table 7: Command Set

Operation	Cycle 1	Cycle 2	Valid During Busy
PAGE READ	00h	30h	No
PAGE READ CACHE MODE START[1]	31h	–	No
PAGE READ CACHE MODE START LAST[1]	3Fh	–	No
READ for INTERNAL DATA MOVE[2]	00h	35h	No
RANDOM DATA READ[3]	05h	E0h	No
READ ID	90h	–	No
READ STATUS	70h	–	Yes
PROGRAM PAGE	80h	10h	No
PROGRAM PAGE CACHE[1]	80h	15h	No
PROGRAM for INTERNAL DATA MOVE[2]	85h	10h	No
RANDOM DATA INPUT for PROGRAM [4]	85h	–	No
BLOCK ERASE	60h	D0h	No
RESET	FFh	–	Yes

Notes: 1. Do not cross die address boundaries when using cache operations. See Tables 4 and 5 for definition of die address boundaries.
2. Do not cross die address boundaries when using READ for INTERNAL DATA MOVE and PROGRAM FOR INTERNAL DATA MOVE. See Tables 4 and 5 for definition of die address boundaries.
3. RANDOM DATA READ command limited to use within a single page.
4. RANDOM DATA INPUT for PROGRAM command limited to use within a single page.

READ Operations

PAGE READ 00h-30h

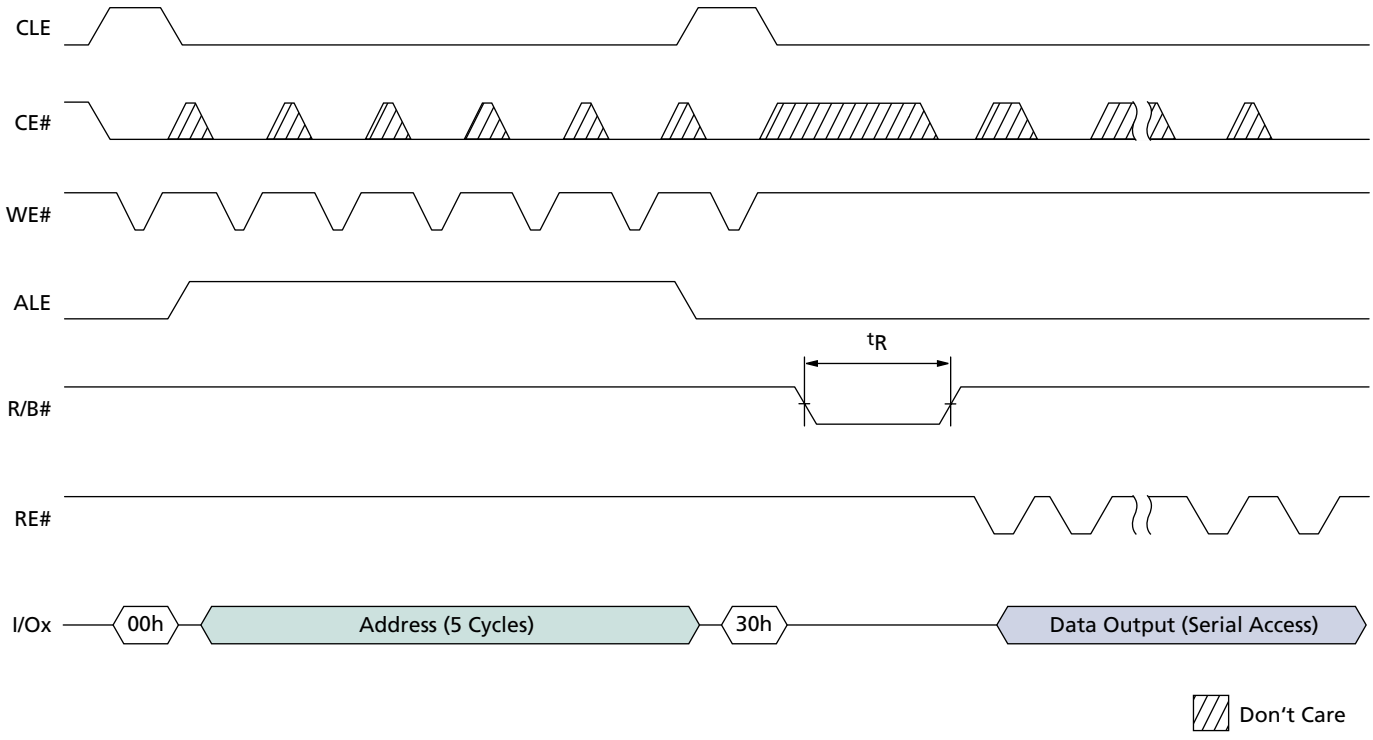
On initial power up, each device defaults to read mode. To enter the read mode while in operation, write the 00h-30h command sequence to the command register along with the five ADDRESS cycles.

Writing 00h to the command register starts the ADDRESS LATCH cycle. Five ADDRESS cycles are input next. Finally the 30h command is loaded into the command register.

While monitoring the read status to determine when the ^{t}R (transfer from Flash array to data register) is complete, the user must re-issue the READ (00h) command to make the change from STATUS to DATA. (See Figure 44 on page 48 and Figure 45 on page 49 for examples.) After the READ command has been re-issued, pulsing the RE# line will result in outputting data, starting from the initial column address.

A serial page read sequence outputs a complete page of data. After 30h is written, the page data is transferred to the data register, and R/B# goes LOW during the transfer. When the transfer to the data register is complete, R/B# returns HIGH. At this point, data can be read from the device. Starting from the initial column address to the end of the page, read the data by repeatedly pulsing RE# at the maximum ^{t}RC rate. (See Figure 18 on page 23.)

Figure 18: PAGE READ Operation



RANDOM DATA READ 05h-E0h

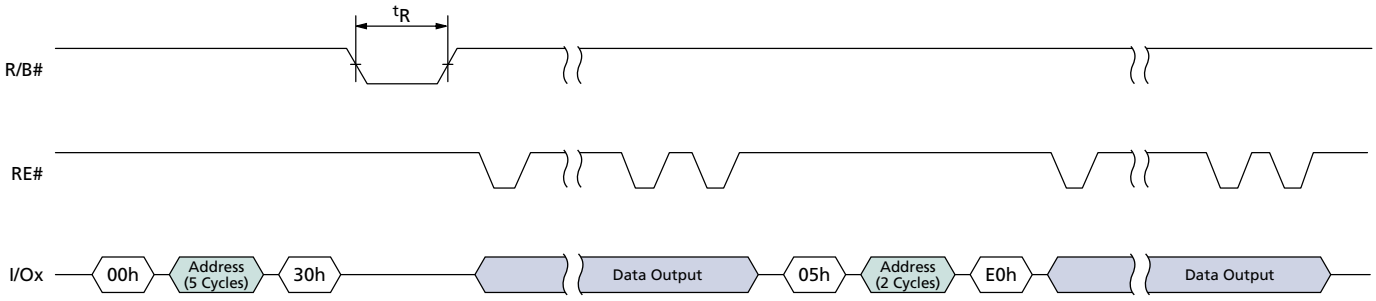
The RANDOM DATA READ command enables the user to specify a new column address so the data at single or multiple addresses can be read. The random read mode is enabled after a normal PAGE READ (00h-30h sequence).

Random data can be output after the initial page read by writing an 05h-E0h command sequence along with the new column address (two cycles).

The RANDOM DATA READ command can be issued without limit within the page.

Only data on the current page can be read. Pulsing the RE# pin outputs data sequentially. See Figure 19 on page 24.

Figure 19: RANDOM DATA READ Operation



PAGE READ CACHE MODE START 31h; PAGE READ CACHE MODE START LAST 3Fh

Micron NAND Flash devices have a cache register that can be used to increase READ operation speed when accessing sequential pages in a block.

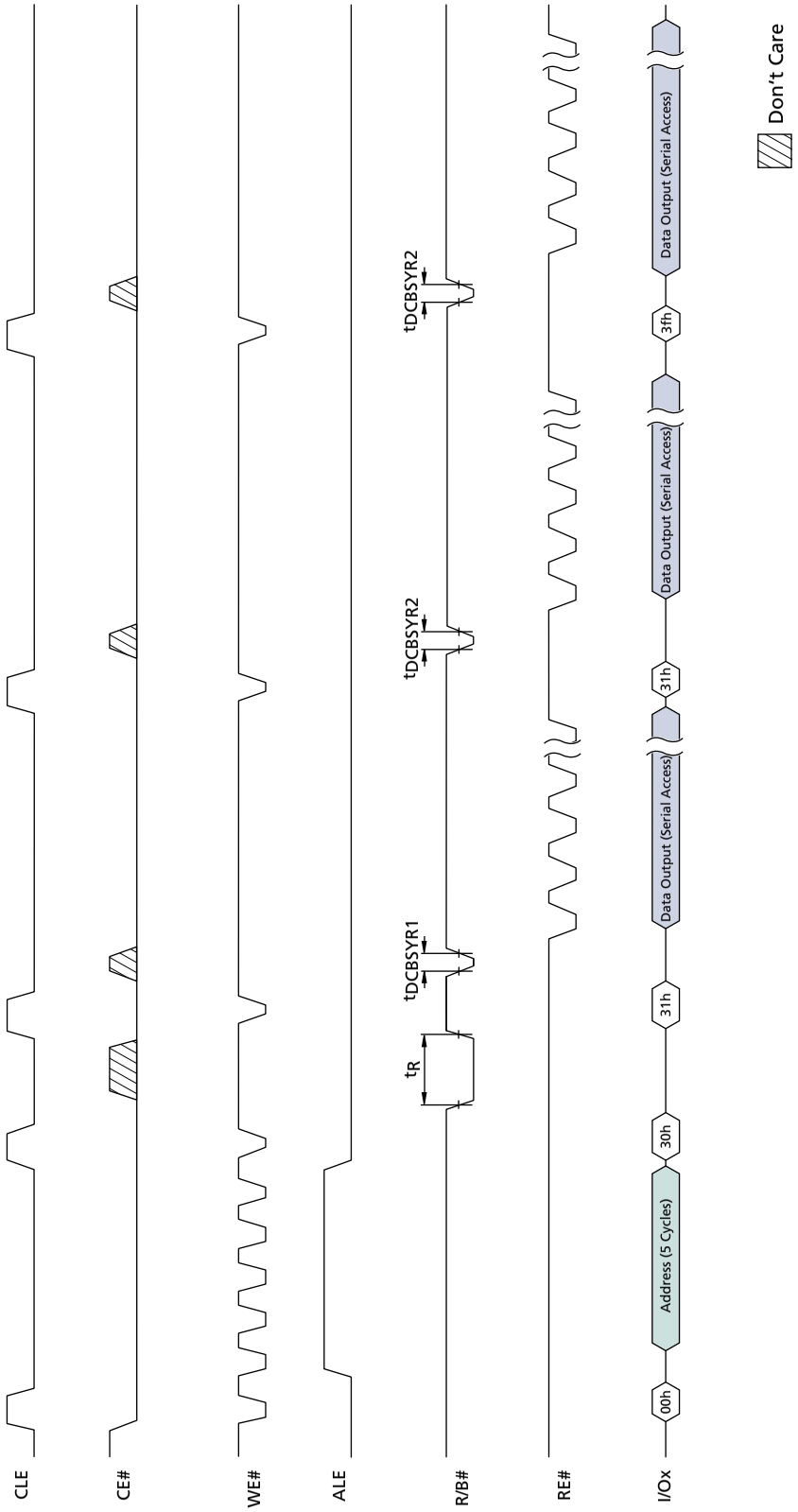
First, a normal PAGE READ (00h-30h) command sequence is issued. (See Figure 20 on page 25 for operation details.) The R/B# signal goes LOW for ^{t}R during the time it takes to transfer the first page of data from the memory to the data register. After R/B# returns to HIGH, the PAGE READ CACHE MODE START (31h) command is latched into the command register. R/B# goes LOW for ^{t}DCBSYR1 while data is being transferred from the data register to the cache register. Once the data register contents are transferred to the cache register, another PAGE READ is automatically started as part of the 31h command. Data is transferred from the next sequential page of the memory array to the data register during the same time data is being read serially (pulsing of RE#) from the cache register. If the total time to output data exceeds ^{t}R, then the PAGE READ is hidden.

The second and subsequent pages of data are transferred to the cache register by issuing additional 31h commands. R/B# will stay LOW up to ^{t}DCBSYR2. This time can vary, depending on whether the previous memory-to-data-register transfer was completed prior to issuing the next 31h command. If the data transfer from memory to the data register is not completed before the 31h command is issued, R/B# stays LOW until the transfer is complete.

It is not necessary to output a whole page of data before issuing another 31h command. R/B# will stay LOW until the previous PAGE READ is complete and the data has been transferred to the cache register.

To read out the last page of data, the PAGE READ CACHE MODE START LAST (3Fh) command is issued. This command transfers data from the data register to the cache register without issuing another PAGE READ. (See Figure 20 on page 25.)

Figure 20: PAGE READ CACHE MODE

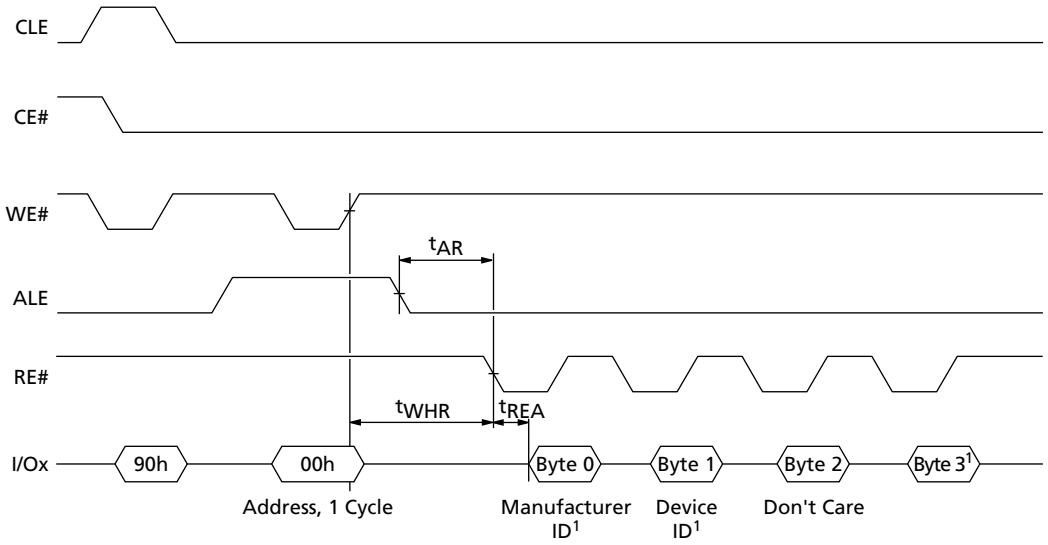


READ ID 90h

The READ ID command is used to read the 4 bytes of identifier codes programmed into the devices. The READ ID command reads a 4-byte table that includes Manufacturer's ID, device configuration, and part-specific information. See Table 8 on page 27, which shows complete listings of all configuration details.

Writing 90h to the command register puts the device into the read ID mode. The command register stays in this mode until another valid command is issued. (See Figure 21.)

Figure 21: READ ID Operation



Notes: 1. See Table 8 on page 27.

Table 8: Device ID and Configuration Codes

	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value[1]	Notes
Byte 0	Manufacturer ID										
	Micron	0	0	1	0	1	1	0	0	2Ch	
Byte 1	Device ID										
MT29F2G08AAB	2Gb, x8, 3V	1	1	0	1	1	0	1	0	DAh	
MT29F2G16AAB	2Gb, x16, 3V	1	1	0	0	1	0	1	0	CAh	
MT29F4G08BAB	4Gb, x8, 3V	1	1	0	1	1	1	0	0	DCh	
MT29F4G16BAB	4Gb, x16, 3V	1	1	0	0	1	1	0	0	CCh	
MT29F8G08FAB	8Gb, x8, 3V	1	1	0	1	1	1	0	0	DCh	2
Byte 2											
Byte value	Don't Care	x	x	x	x	x	x	x	x	XXh	
Byte 3											
Page size	2KB							0	1	01b	
Spare area size (bytes)	64					0	1			01b	
Block size (w/o spare)	128KB			0	1					01b	
Organization	x8		0							0b	
	x16		1							1b	
Reserved		0								0b	
Byte value	x8	0	0	0	1	0	1	0	1	15h	
Byte value	x16	0	1	0	1	0	1	0	1	55h	

Notes: 1. b = binary, h = hex
2. The MT29F8G08FAB device ID code reflects the configuration of each 4Gb section.

READ STATUS 70h

These NAND Flash devices have an 8-bit status register that the software can read during device operation. On the x16 device, I/O[15:8] are "0" when reading the status register. Table 9 on page 28 describes the status register.

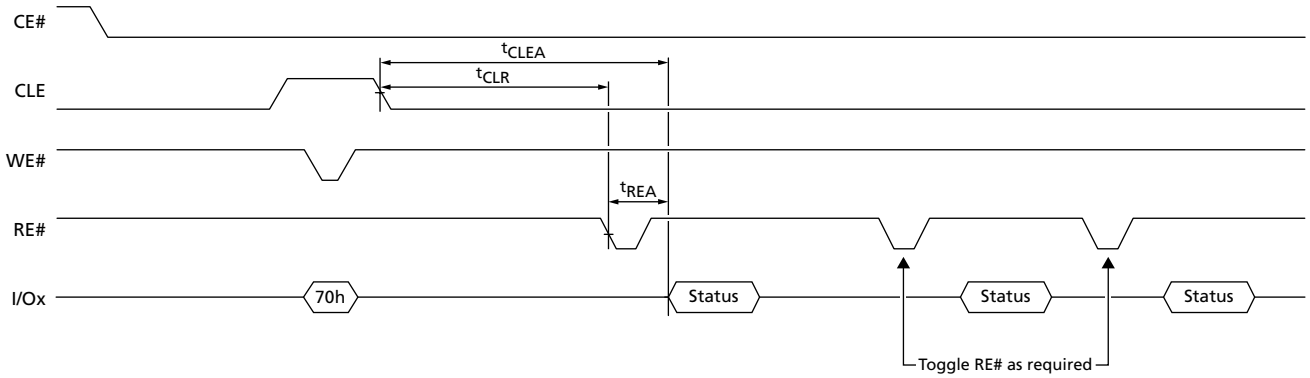
After the READ STATUS command has been issued to the NAND Flash device, all subsequent READ cycles will output data from the status register until another command is issued. Note that the RE# pin can be toggled multiple times without issuing a new READ STATUS command, as shown in Figure 21. Each time the RE# pin is toggled, the updated status will be output on I/O[7:0].

In addition, after a READ STATUS command has been issued to the NAND Flash device, the status register provides continually updated output on I/O[7:0] as long as CE# and RE# are held LOW, i.e., RE# does not have to be toggled.

Note that MT29FxGxxxAB devices do *not* support a READ STATUS operation in which the READ STATUS (70h) command is repeatedly issued after each RE# toggle.

Additional details regarding READ STATUS implementation are available in Micron technical note TN-29-13 at: www.micron.com/products/nand/massstorage/technote.

Figure 22: Status Register Operation



While monitoring the read status to determine when the tR (transfer from Flash array to data register) is complete, the user must re-issue the READ (00h) command to make the change from STATUS to DATA. After the READ command has been re-issued, pulsing the RE# line will output data, starting from the initial column address.

Table 9: Status Register Bit Definition

SR Bit	Page Program	Program Page Cache Mode	Page Read	Page Read Cache Mode	Block Erase	Definition
0	Pass/fail	Pass/fail (N)	–	–	Pass/fail	"0" = Successful PROGRAM/ERASE "1" = Error in PROGRAM/ERASE
1	–	Pass/fail (N-1)	–	–	–	"0" = Successful PROGRAM/ERASE "1" = Error in PROGRAM/ERASE
2	–	–	–	–	–	"0"
3	–	–	–	–	–	"0"
4	–	–	–	–	–	"0"
5	Ready/busy	Ready/busy[1]	Ready/busy	Ready/busy[1]	Ready/busy	"0" = Busy "1" = Ready
6	Ready/busy	Ready/busy cache[2]	Ready/busy	Ready/busy cache[2]	Ready/busy	"0" = Busy "1" = Ready
7	Write protect	Write protect	Write protect	Write protect	Write protect	"0" = Protected "1" = Not protected
[15:8]	–	–	–	–	–	"0"

Notes: 1. Status register bit 5 is "0" during the actual programming operation. If cache mode is used, this bit will be "1" when all internal operations are complete.
2. Status register bit 6 is "1" when the cache is ready to accept new data. R/B# follows bit 6. See Figure 20 on page 25, and Figure 25 on page 30.

PROGRAM Operations

PROGRAM PAGE 80h-10h

Micron NAND Flash devices are inherently page-programmed devices. Within a block, the pages must be programmed consecutively from the least significant bit (LSB) page of the block to most significant bit (MSB) pages of the block. Random page address programming is prohibited.

Micron NAND flash devices also support partial-page programming operations. This means that any single bit can only be programmed one time before an erase is required; however, the page can be partitioned such that a maximum of eight programming operations are allowed before an erase is required.

SERIAL DATA INPUT 80h

PAGE PROGRAM operations require loading the SERIAL DATA INPUT (80h) command into the command register, followed by five ADDRESS cycles, then the data. Serial data is loaded on consecutive WE# cycles starting at the given address. The PROGRAM (10h) command is written after the data input is complete. The internal write state machine automatically executes the proper algorithm and controls all the necessary timing to program and verify the operation. Write verification only detects "1s" that are not successfully written to "0s."

R/B# goes LOW for the duration of array programming time, ^{t}PROG. The READ STATUS REGISTER (70h) command and the RESET (FFh) command are the only commands valid during the programming operation. Bit 6 of the status register will reflect the state of R/B#. When the device reaches ready, read bit 0 of the status register to determine if the program operation passed or failed. (See Figure 23.) The command register stays in read status register mode until another valid command is written to it.

RANDOM DATA INPUT 85h

After the initial data set is input, additional data can be written to a new column address with the RANDOM DATA INPUT (85h) command. The RANDOM DATA INPUT command can be used any number of times in the same page prior to issuing the PAGE WRITE (10h) command. See Figure 24 for the proper command sequence.

Figure 23: PROGRAM and READ STATUS Operation

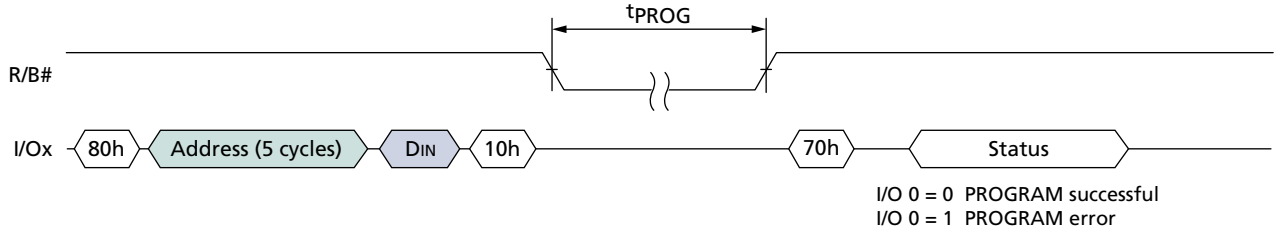
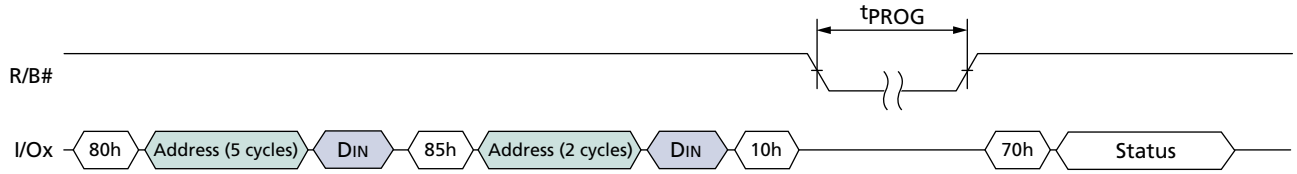


Figure 24: RANDOM DATA INPUT



PROGRAM PAGE CACHE MODE 80h-15h

Cache programming is actually a buffered programming mode of the standard PAGE PROGRAM command. Programming is started by loading the SERIAL DATA INPUT (80h) command to the command register, followed by five cycles of address, and a full or partial page of data. The data is initially copied into the cache register, and the CACHE WRITE (15h) command is then latched to the command register. Data is transferred from the cache register to the data register on the rising edge of WE#. R/B# goes LOW during this transfer time. After the data has been copied into the data register and R/B# returns to HIGH, memory array programming begins.

When R/B# returns to HIGH, new data can be written to the cache register by issuing another CACHE PROGRAM command sequence. The time that R/B# stays LOW will be controlled by the actual programming time. The first time through equals the time it takes to transfer the cache register contents to the data register. On the second and subsequent programming passes, transfer from the cache register to the data register is held off until current data register content has been programmed into the array.

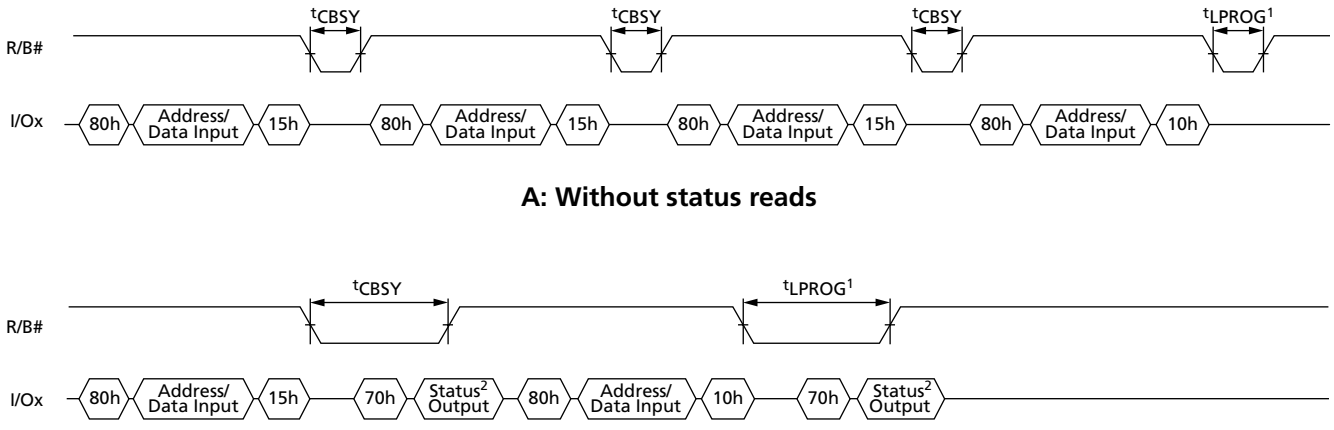
Bit 6 (Cache R/B#) of the status register can be read by issuing the READ STATUS (70h) command to determine when the cache register is ready to accept new data. The R/B# pin always follows bit 6.

Bit 5 (R/B#) of the status register can be polled to determine when the actual programming of the array is complete for the current programming cycle.

If just the R/B# pin is used to determine programming completion, the last page of the program sequence must use the PROGRAM PAGE (10h) command instead of the CACHE PROGRAM (15h) command. If the CACHE PROGRAM (15h) command is used every time, including the last page of the programming sequence, status register bit 5 must be used to determine when programming is complete. (See Figure 25.)

Bit 0 of the status register returns the pass/fail for the previous page when bit 6 of the status register is a "1" (ready state). The pass/fail status of the current PROGRAM operation is returned with bit 0 of the status register when bit 5 of the status register is a "1" (ready state). (See Figure 25.)

Figure 25: PROGRAM PAGE CACHE MODE Example



Notes: 1. See Note 3, Table 19 on page 41.
2. Check I/O[6:5] for internal Ready/Busy. Check I/O[1:0] for pass fail. RE# can stay LOW or pulse multiple times after a 70h command.

Internal Data Move

An internal data move requires two command sequences. Issue a READ for INTERNAL DATA MOVE (00h-35h) command first, then the INTERNAL DATA MOVE (85h-10h) command. Data moves are only supported within the die from which data is read.

READ FOR INTERNAL DATA MOVE 00h-35h

This READ command is used in conjunction with the INTERNAL DATA MOVE (85h-10h) command. First, (00h) is written to the command register, then the internal source address is written (five cycles). After the address is input, the READ for INTERNAL DATA MOVE (35h) command writes to the command register. This transfers a page from memory into the cache register.

The written column addresses are ignored even though all five ADDRESS cycles are required.

The memory device is now ready to accept the INTERNAL DATA MOVE (85h-10h) command. Please refer to the description of this command in the following section.

INTERNAL DATA MOVE 85h-10h

After the READ for INTERNAL DATA MOVE command has been issued and R/B# goes HIGH, the INTERNAL DATA MOVE command can be written to the command register. This command transfers the data from the cache register to the data register and programming of the new destination page begins. After the INTERNAL DATA MOVE command and address sequence are written to the device, R/B# goes LOW while the internal control logic automatically programs the new page. The READ STATUS command and bit 6 of the status register can be used instead of the R/B# line to determine when the write is complete. Bit 0 of the status register indicates if the operation was successful.

The RANDOM DATA INPUT (85h) command can be used during the INTERNAL DATA MOVE command sequence to modify a word or multiple words of the original data. First, data is copied into the cache register using the 00h-35h command sequence, then the RANDOM DATA INPUT (85h) command is written along with the address of the data to be modified next. New data is input on the external data pins. This copies the new data into the cache register.

When 10h is written to the command register, the original data plus the modified data is transferred to the data register, and programming of the new page is started. The RANDOM DATA INPUT command can be issued as many times as necessary before starting the programming sequence with 10h. (See Figures 26 and 27 on page 32.)

Because the INTERNAL DATA MOVE operation does not utilize external memory, ECC cannot be used to check for errors before programming the data to a new page. This can lead to a data error if the source page contains a bit error due to charge loss or charge gain. In the case that multiple INTERNAL DATA MOVE operations are performed, these bit errors may accumulate without correction. For this reason, it is highly recommended that systems utilizing the INTERNAL DATA MOVE operation use a robust ECC scheme that can correct two or more bits per sector.

Figure 26: INTERNAL DATA MOVE

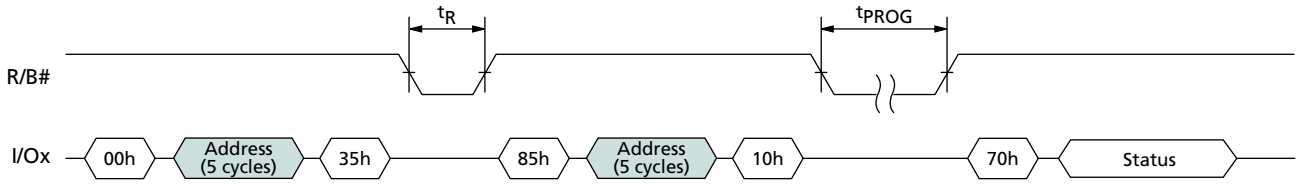
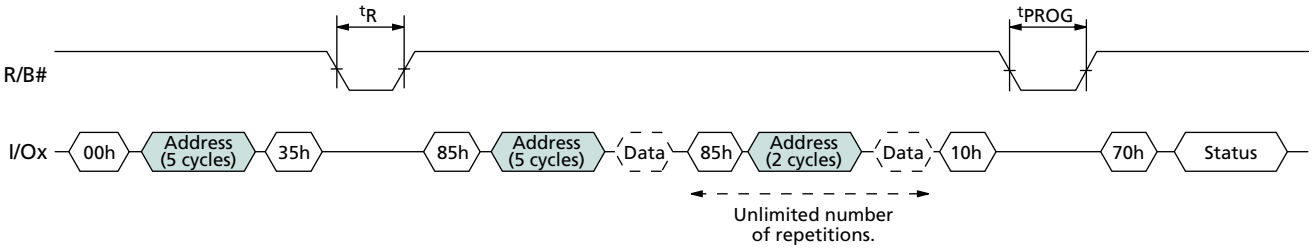


Figure 27: INTERNAL DATA MOVE with RANDOM DATA INPUT



BLOCK ERASE Operation

BLOCK ERASE 60h-D0h

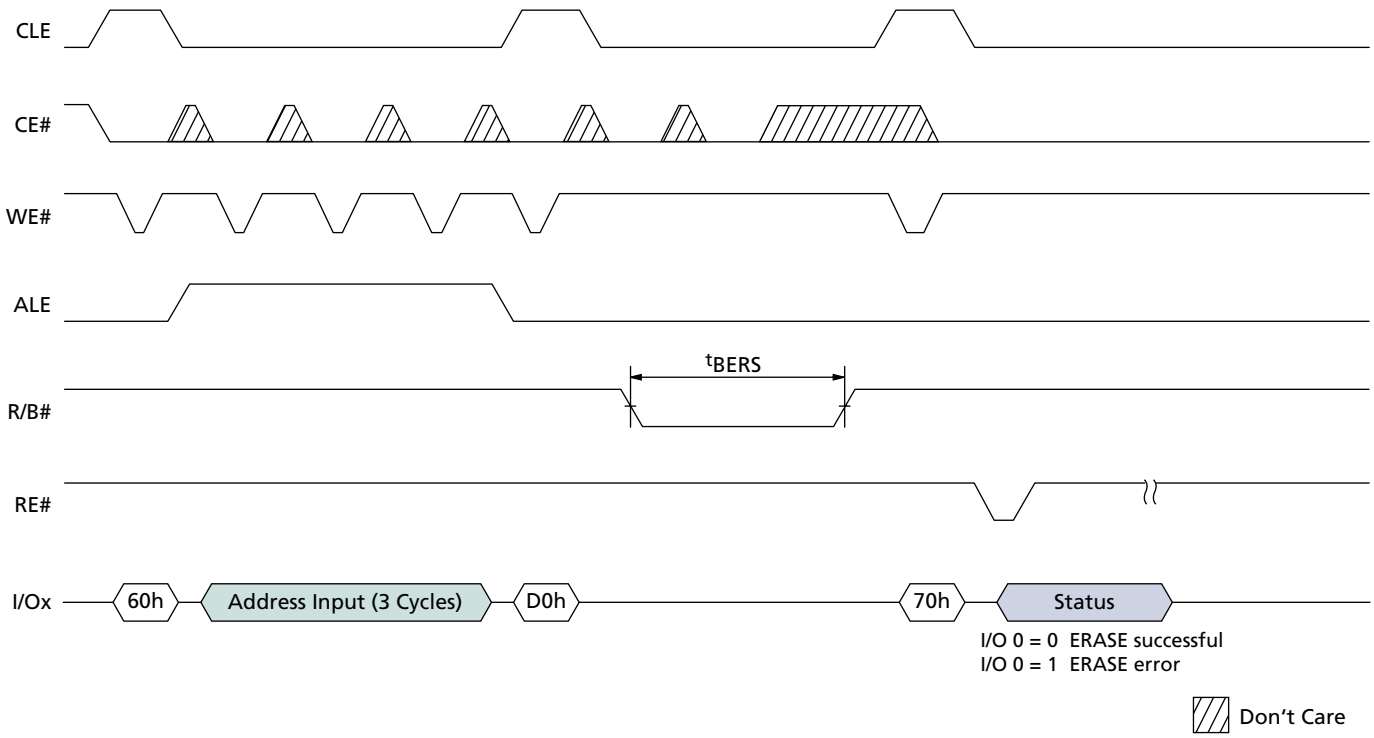
Erasing occurs at the block level. For example, the MT29F2G08xxB device has 2,048 erase blocks organized as 64 2,112-byte (2,048 + 64 bytes) pages per block. Each block is 132K bytes (128K + 4K bytes). The BLOCK ERASE command operates on one block at a time. (See Figure 28.)

Three cycles of addresses A[28:18] are required for the x8 device, and three cycles of addresses [27:17] are required for the x16 device. Although addresses A[17:12] (x8) and A[16:11] (x16) are loaded, they are a "Don't Care" and are ignored for BLOCK ERASE operations. (See Figures 5 and 6 on page 11 for addressing details.)

The actual command sequence is a two-step process. The ERASE SETUP (60h) command is first written to the command register. Then three cycles of addresses are written to the device. Next, the ERASE CONFIRM (D0h) command is written to the command register. At the rising edge of WE#, R/B# goes LOW and the internal write state machine automatically controls the timing and erase-verify operations. R/B# stays LOW for the entire ^{t}BERS erase time.

The READ STATUS REGISTER command can be used to check the status of the ERASE operation. When bit 6 = "1" the erase operation is complete. Bit 0 indicates a pass/fail condition where "0" = pass. (See Figure 28, and Table 9 on page 28.)

Figure 28: BLOCK ERASE Operation



RESET Operation

RESET FFh

The RESET command is used to put the memory device into a known condition and to abort a command sequence in progress.

RANDOM READ, PROGRAM, and ERASE commands can be aborted while the device is in the busy state. The contents of the memory location being programmed or the block being erased are no longer valid. The data may be partially erased or programmed, and is invalid. The command register is cleared and is ready for the next command.

The status register contains the value E0h when WP# is HIGH; otherwise it is written with a 60h value. R/B# goes low for ^{t}RST after the RESET command is written to the command register. (See Figure 29 and Table 10.)

Figure 29: RESET Operation

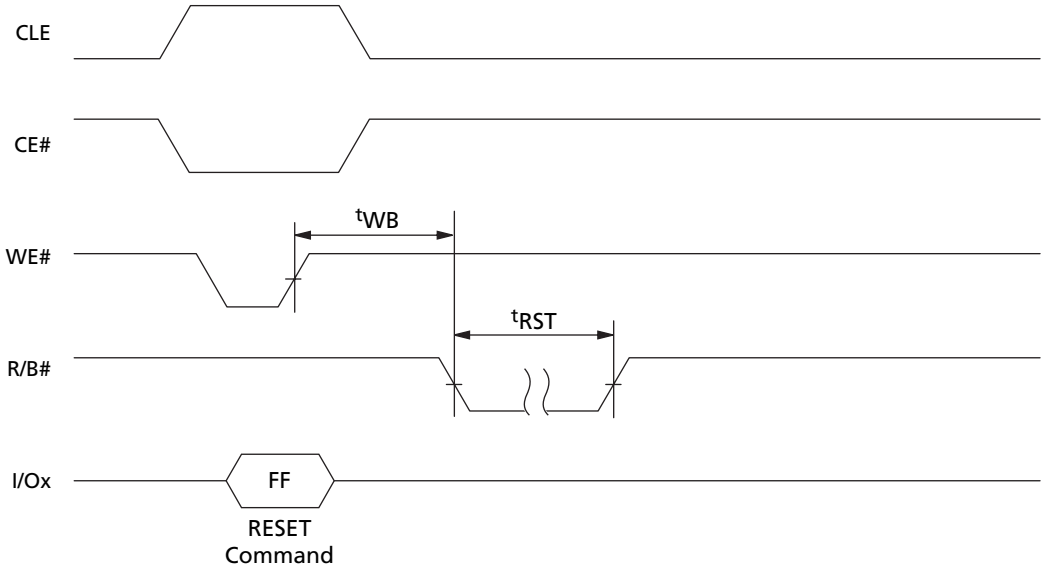


Table 10: Status Register Contents After RESET Operation

Condition	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
WP# HIGH	Ready	1	1	1	0	0	0	0	0	E0h
WP# LOW	Ready and write protected	0	1	1	0	0	0	0	0	60h

WRITE PROTECT Operation

The WRITE PROTECT feature protects the device against inadvertent PROGRAM and ERASE operations. All PROGRAM and ERASE operations are disabled when WP# is LOW. For WRITE PROTECT timing details, see Figures 30 through 33.

Figure 30: ERASE Enable

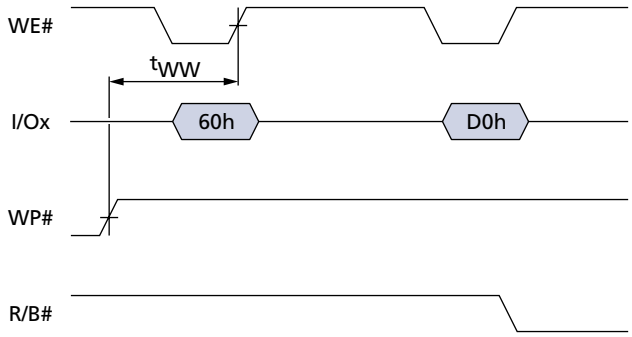


Figure 31: ERASE Disable

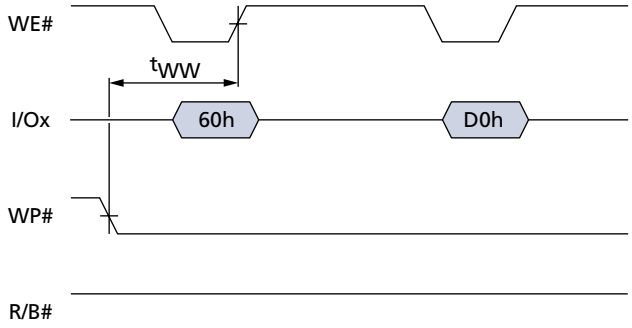


Figure 32: PROGRAM Enable

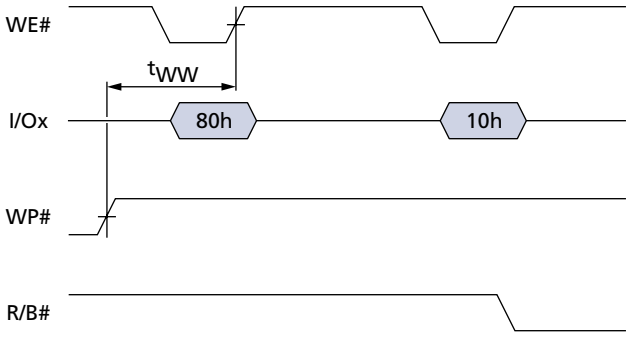
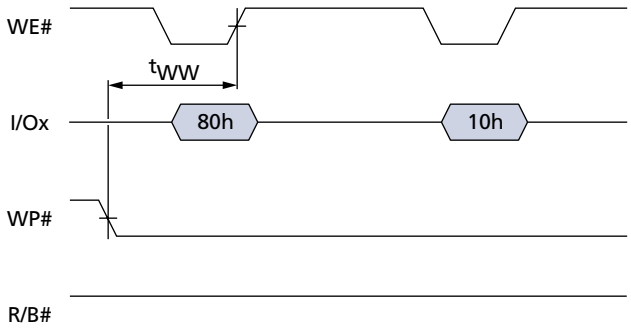


Figure 33: PROGRAM Disable



Error Management

Micron NAND devices are specified to have a minimum of 2,008 (NVB) valid blocks out of every 2,048 total available blocks. This means the devices may have blocks that are invalid when they are shipped. An invalid block is one that contains one or more bad bits. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below NVB during the endurance life of the product.

Although NAND memory devices may contain bad blocks, they can be used quite reliably in systems that provide bad-block mapping, replacement, and error correction algorithms. This type of software environment ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the Flash device.

The first block (physical block address 00h) for each CE# in Micron NAND devices is guaranteed to be free of defects (up to 1,000 PROGRAM/ERASE cycles) when shipped from the factory. This provides a reliable location for storing boot code and critical boot information.

Before NAND Flash devices are shipped from Micron, they are erased. The factory identifies invalid blocks before shipping by programming data other than FFh (x8) or FFFFh (x16) into the first spare location (column address 2,048 for x8 devices, or 1,024 for x16 devices) of the first or second page of each bad block.

System software should check the first spare address on the first or second page of each block prior to performing any erase or programming operations on the Flash device. A bad block table can then be created, allowing system software to map around these areas. Factory testing is performed under worst-case conditions. Because blocks marked "bad" may be marginal, it may not be possible to recover this information if the block is erased.

Over time, some memory locations may fail to program or erase properly. In order to ensure that data is stored properly over the life of the Flash device, certain precautions must be taken, such as:

- Always check status after a WRITE, ERASE, or DATA MOVE operation.
- Use some type of error detection and correction algorithm to recover from single-bit errors.
- Use a bad-block replacement algorithm.

Electrical Characteristics

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating *only,* and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 11: Absolute Maximum Ratings by Device

Device	Symbol		Min	Max	Unit
MT29FxGxxxAx	VIN	Supply voltage on any pin relative to Vss	–0.6	+4.6	V
MT29FxGxxxAx	VCC				
Storage temperature	TSTG		–65	+150	°C
Short circuit output current, I/Os				5	mA

Table 12: Recommended Operating Conditions

Parameter/Condition		Symbol	Min	Typ	Max	Unit
Operating temperature	Commercial	^{t}A	0	–	+70	°C
	Extended	^{t}A	–40	–	+85	°C
VCC supply voltage		Vcc	2.7	3.3	3.6	V
Supply voltage		Vss	0	0	0	V

Vcc Power Cycling

Micron NAND Flash devices are designed to prevent data corruption during power transitions. VCC is internally monitored. When VCC goes below 2.0V, PROGRAM and ERASE functions are disabled. WP# provides additional hardware protection. WP# should be kept at VIL during power cycling. When VCC reaches 2.0V, a minimum of 10µs should be allowed for the Flash to initialize before executing any commands. (See Figure 17 on page 21.)

Table 13: DC and Operating Characteristics

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Sequential read current	^{t}CYCLE = 30ns, CE# = VIL, IOUT = 0mA	ICC1	–	15	30	mA
Program current	–	ICC2	–	15	30	mA
Erase current	–	ICC3	–	15	30	mA
Standby current (TTL)	CE# = VIH, PRE = WP# = 0V/VCC	ISB1	–	–	1	mA
Standby current (CMOS) MT29F2GxxAAB	CE# = VCC - 0.2V, PRE = WP# = 0V/VCC	ISB2	–	10	50	µA
Standby current (CMOS) MT29F4GxxBAB MT29F8G08FAB	CE# = VCC - 0.2V, PRE = WP# = 0V/VCC	ISB2	–	20	100	µA
Input leakage current	VIN = 0V to VCC	ILI	–	–	±10	µA
Output leakage current	VOUT = 0V to VCC	ILO	–	–	±10	µA
Input high voltage	I/O [7–0], I/O [15–0] CE#, CLE, ALE, WE#, RE#, WP#, PRE, R/B#	VIH	0.8 x VCC	–	VCC + 0.3	V
Input low voltage (all inputs)	–	VIL	-0.3	–	0.8	V
Output high voltage	IOH = -400µA	VOH	2.4	–	–	V
Output low voltage	IOL = 2.1mA	VOL	–	–	0.4	V
Output low current (R/B#)	VOL = 0.4V	IOL (R/B#)	8	10	–	mA

Note: The PRE function is not supported on extended-temperature devices.

Table 14: Valid Blocks

Parameter	Symbol	Device	Min	Max	Unit	Notes
Number of valid blocks	NVB	MT29F2GxxAAB	2,008	2,048	Blocks	1, 2
		MT29F4GxxBAB	4,016	4,096		
		MT29F8G08FAB	8,032	8,192		

Notes: 1. Invalid blocks are blocks that contain one or more bad bits. The device may contain bad blocks upon shipment. Additional bad blocks may develop over time; however, the total number of available blocks will not drop below NVB during the endurance life of the device. Do not erase or program blocks marked invalid by the factory.
2. Block 00h (the first block) is guaranteed to be valid and does not require error correction up to 1,000 PROGRAM/ERASE cycles.

Table 15: Capacitance

Description	Symbol	Device	Max	Unit	Notes
Input capacitance	CIN	MT29F2GxxAAB	10	pF	1, 2
		MT29F4GxxBAB	20		
		MT29F8G08FAB	40		
Input/output capacitance (I/O)	CIO	MT29F2GxxAAB	10	pF	1, 2
		MT29F4GxxBAB	20		
		MT29F8G08FAB	40		

Notes: 1. These parameters are verified in device characterization and are not 100 percent tested.
2. Test conditions: T_C = 25°C; f = 1 MHz; VIN = 0V.

Table 16: Test Conditions

Parameter		Value	Notes
Input pulse levels: MT29FxGxxxAB		0.0V to 3.3V	
Input rise and fall times		5ns	
Input and output timing levels		Vcc/2	
Output load	MT29FxGxxxAB (Vcc = 3.0V ±10%)	1 TTL GATE and CL = 50pF	
	MT29FxGxxxAB (Vcc = 3.3V ±10%)	1 TTL GATE and CL = 100pF	1

Notes: 1. Verified in device characterization; not 100 percent tested.

Table 17: AC Characteristics: Command, Data, and Address Input

Parameter	Symbol	x16		x8		Unit	Notes
		Min	Max	Min	Max		
ALE to data start	^{t}ADL	100	–	100	–	ns	1
ALE hold time	^{t}ALH	10	–	5	–	ns	2
ALE setup time	^{t}ALS	25	–	10	–	ns	2
CE# hold time	^{t}CH	10	–	5	–	ns	2
CLE hold time	^{t}CLH	10	–	5	–	ns	2
CLE setup time	^{t}CLS	25	–	10	–	ns	2
CE# setup time	^{t}CS	35	–	15	–	ns	2
Data hold time	^{t}DH	10	–	5	–	ns	2
Data setup time	^{t}DS	20	–	10	–	ns	2
Write cycle time	^{t}WC	45	–	30	–	ns	2
WE# pulse width HIGH	^{t}WH	15	–	10	–	ns	2
WE# pulse width	^{t}WP	25	–	15	–	ns	2
WP# setup time	^{t}WW	30	–	30	–	ns	

Notes: 1. Timing for ^{t}ADL begins in the ADDRESS cycle, on the final rising edge of WE#, and ends with the first rising edge of WE# for data input.
2. For PROGRAM PAGE CACHE MODE operations, the x16 AC characteristics apply for both x16 and x8 devices.

Table 18: AC Characteristics: Normal Operation

Parameter	Symbol	x16		x8		Unit	Notes
		Min	Max	Min	Max		
ALE to RE# delay	^{t}AR	10	–	10		ns	
CE# access time	^{t}CEA	–	45	–	23	ns	1
CE# HIGH to output High-Z	^{t}CHZ	–	20	–	20	ns	2
CLE access time	^{t}CLEA	–	45	–	28	ns	1
CLE to RE# delay	^{t}CLR	10	–	10	–	ns	
Cache busy in page read cache mode (first 31h)	^{t}DCBSYR1	–	3	–	3	µs	
Cache busy in page read cache mode (next 31h and 3Fh)	^{t}DCBSYR2	^{t}DCBSYR1	25	^{t}DCBSYR1	25	µs	
Ouput High-Z to RE# LOW	^{t}IR	0	–	0	–	ns	1
Data output hold time	^{t}OH	15	–	15	–	ns	
Data transfer from Flash array to data register	^{t}R	–	25	–	25	µs	
READ cycle time	^{t}RC	50	–	30	–	ns	1
RE# access time	^{t}REA	–	30	–	18	ns	1
RE# HIGH hold time	^{t}REH	15	–	10	–	ns	1
RE# HIGH to output High-Z	^{t}RHZ	–	30	–	30	ns	2
RE# pulse width	^{t}RP	25	–	15	–	ns	1
Data transfer from Flash array to data register at power-up with PRE enabled @ 3.3V Vcc	^{t}RPRE	–	25	–	25	µs	3
Ready to RE# LOW	^{t}RR	20	–	20	–	ns	
Reset time (READ/PROGRAM/ERASE)	^{t}RST	–	5/10/500	–	5/10/500	µs	4
WE# HIGH to busy	^{t}WB	–	100	–	100	ns	4, 5
WE# HIGH to RE# LOW	^{t}WHR	60	–	60	–	ns	

Notes: 1. For PROGRAM PAGE CACHE MODE operations, the x16 AC Characteristics apply for both x16 and x8 devices.
2. Transition is measured ±200mV from steady-state voltage with load. This parameter is sampled and not 100 percent tested.
3. The PRE function is not supported on extended-temperature devices.
4. If RESET (FFh) command is loaded at ready state, the device goes busy for maximum 5µs.
5. Do not issue a new command during ^{t}WB, even if R/B# is ready.

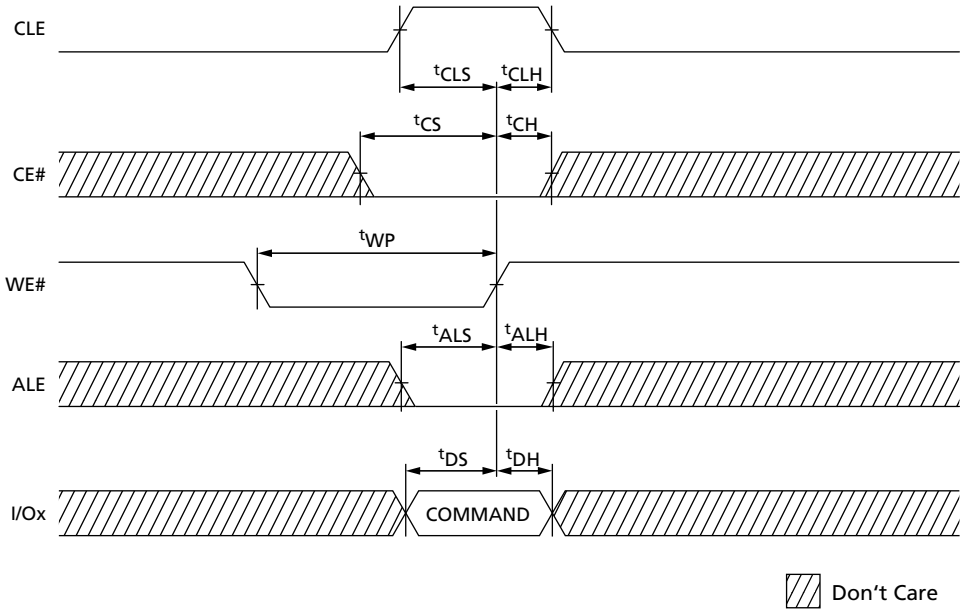
Table 19: PROGRAM/ERASE Characteristics

Parameter	Symbol	Typ	Max	Unit	Notes
Number of partial page programs	NOP	–	8	Cycle	1
Block erase time	^{t}BERS	2	3	ms	
Busy time for cache program	^{t}CBSY	3	700	µs	2
Last page program time	^{t}LPROG	–	–	–	3
Page program time	^{t}PROG	300	700	µs	

Notes: 1. Eight total to the same page.
2. ^{t}CBSY MAX time depends on timing between internal program completion and data in.
3. ^{t}LPROG = ^{t}PROG (last page) + ^{t}PROG (last – 1 page) – cmd load time (last page) – addr load time (last page) – data load time (last page).

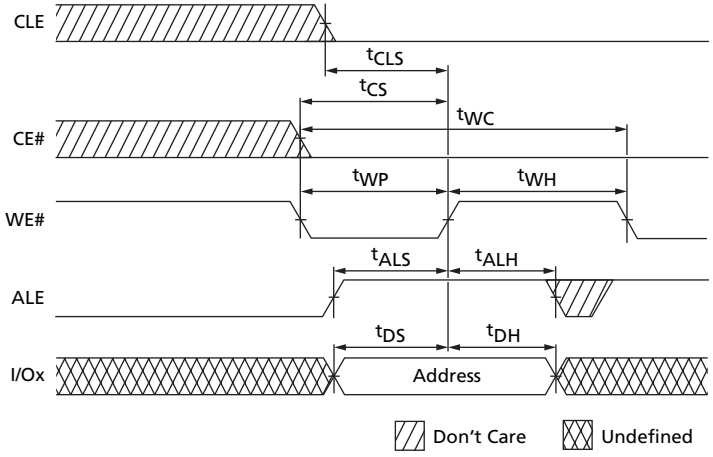
Timing Diagrams

Figure 34: COMMAND LATCH Cycle



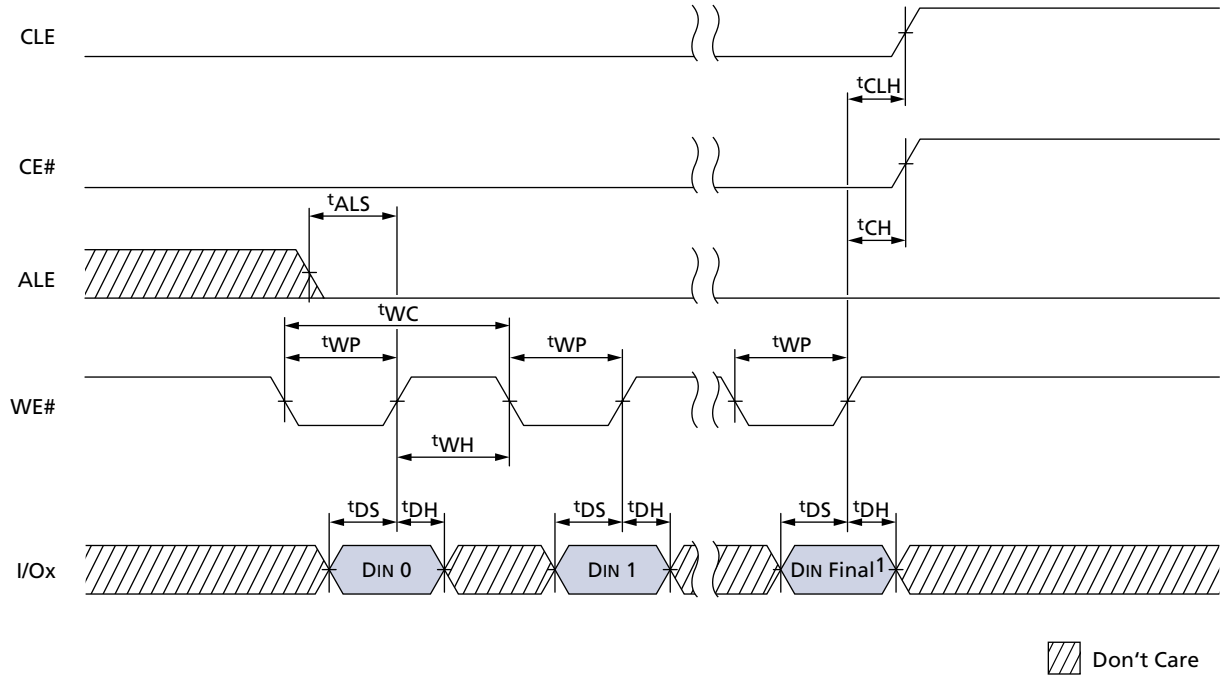
Note: x16: I/O[15:8] must be set to "0.

Figure 35: ADDRESS LATCH Cycle



Note: x16: I/O [15:8] must be set to "0."

Figure 36: INPUT DATA LATCH



Notes: 1. DIN Final = 2,111 (x8) or 1,055 (x16).

Figure 37: SERIAL ACCESS Cycle After READ

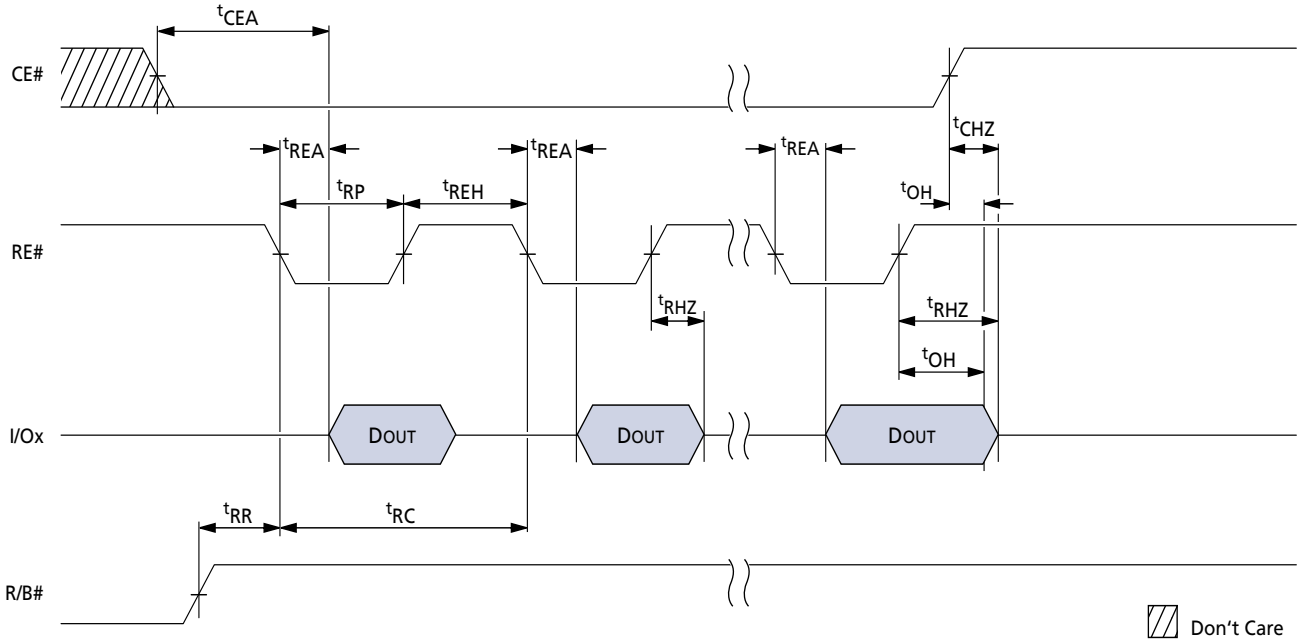


Figure 38: STATUS READ Cycle

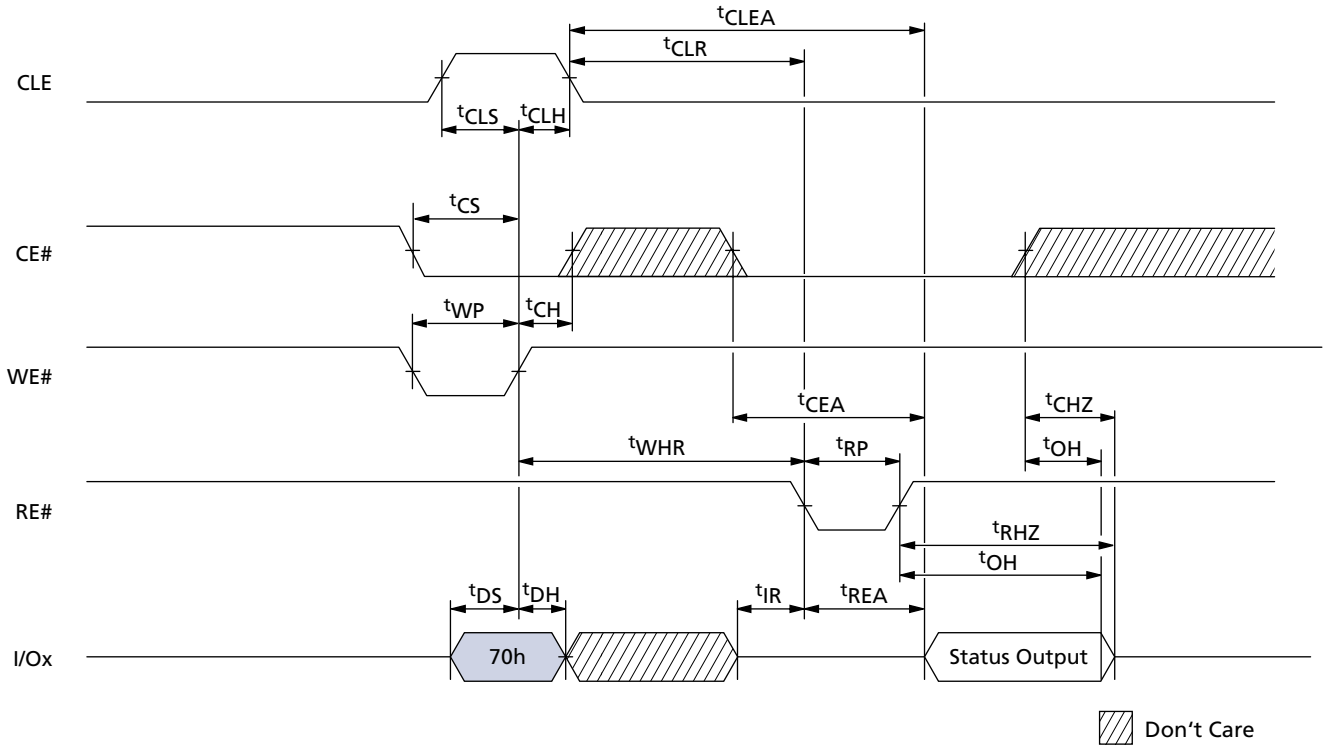


Figure 39: PAGE READ

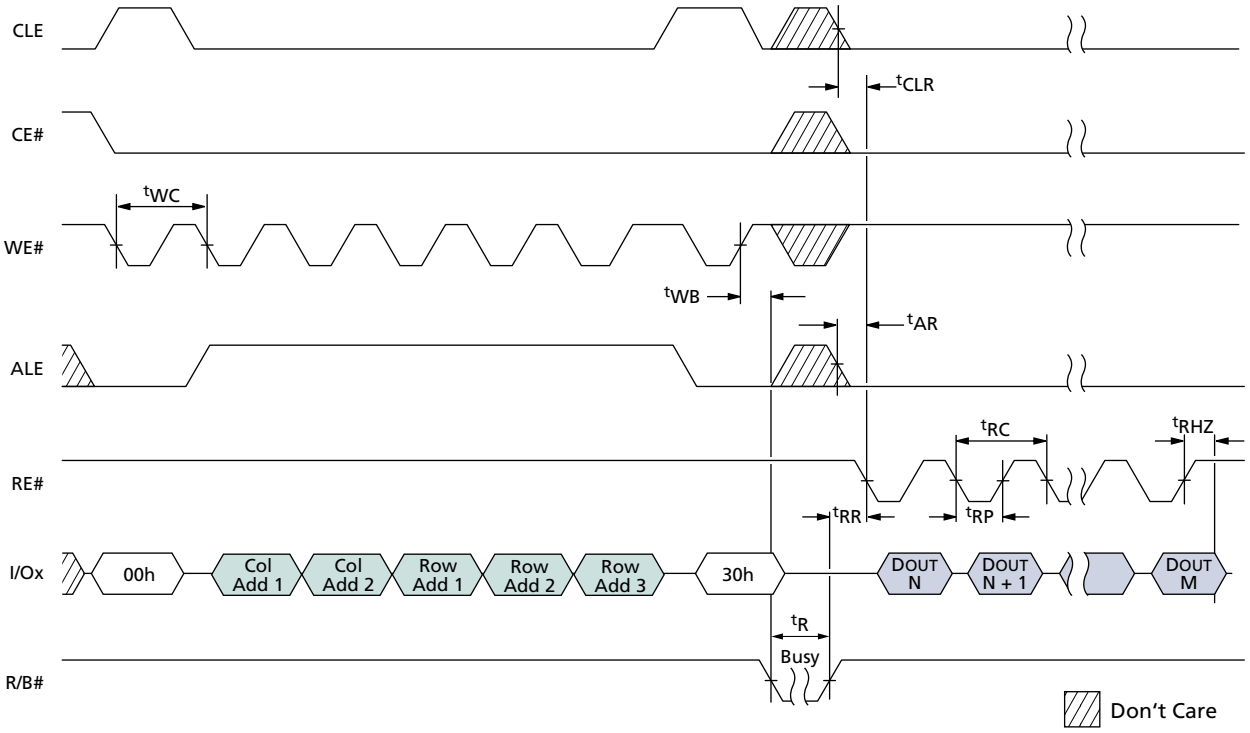


Figure 40: READ Operation with CE# "Don't Care"

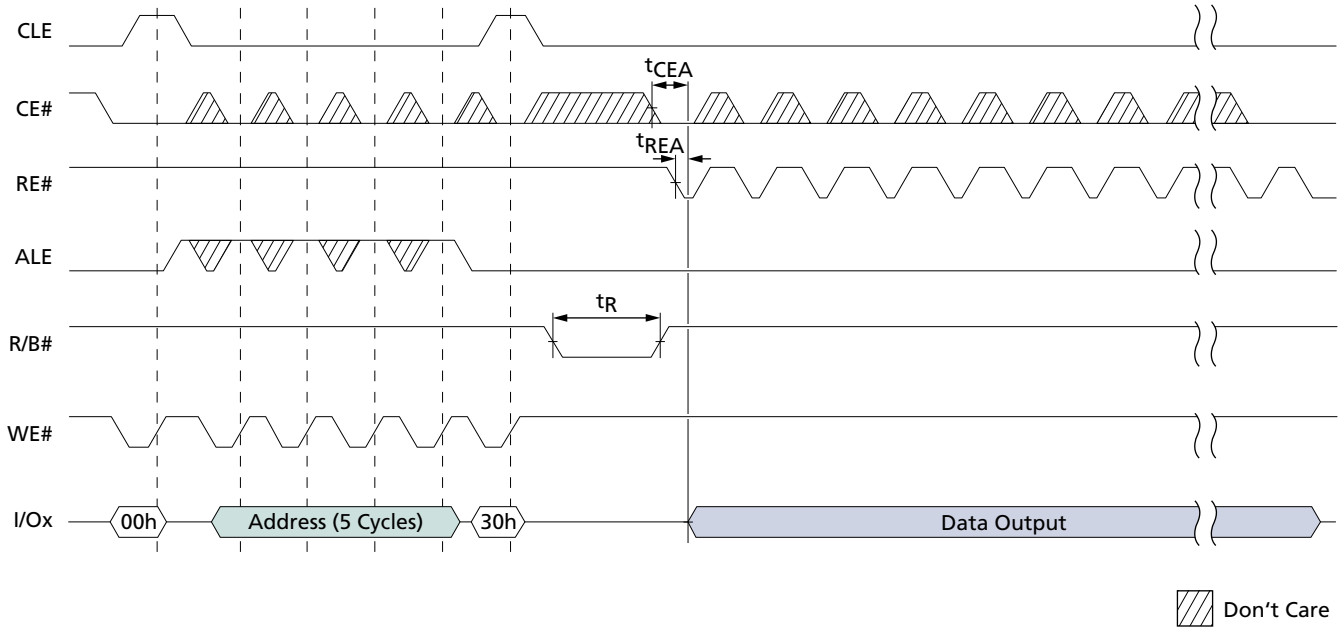
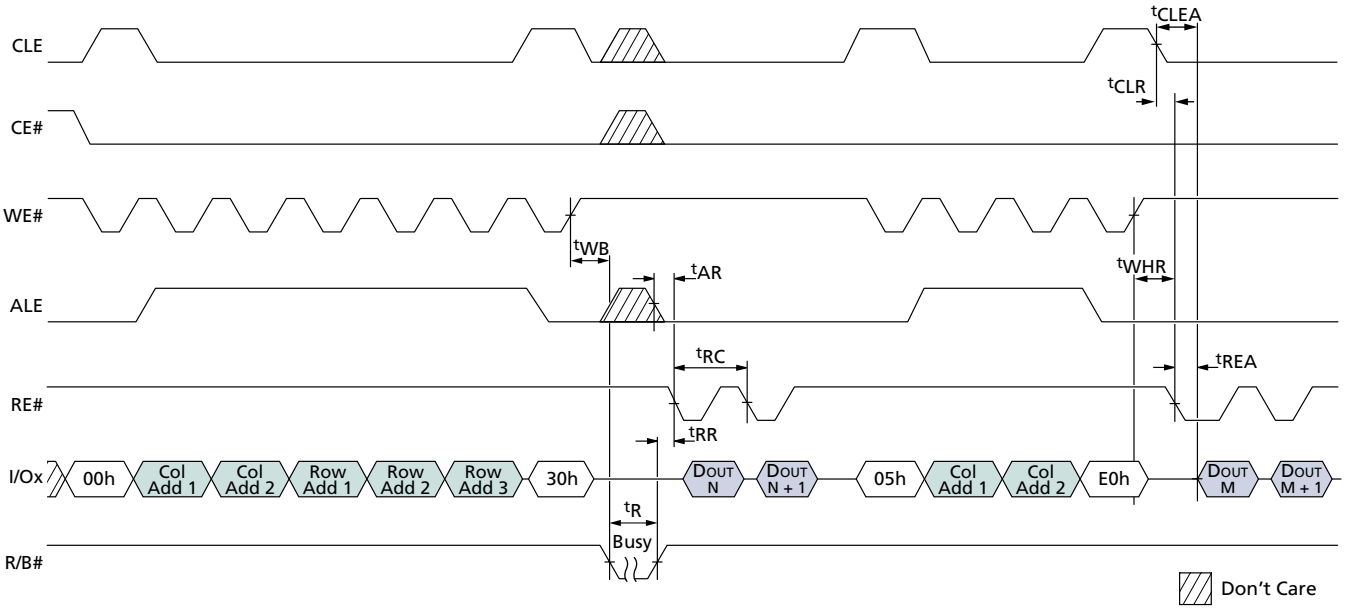


Figure 41: RANDOM DATA READ



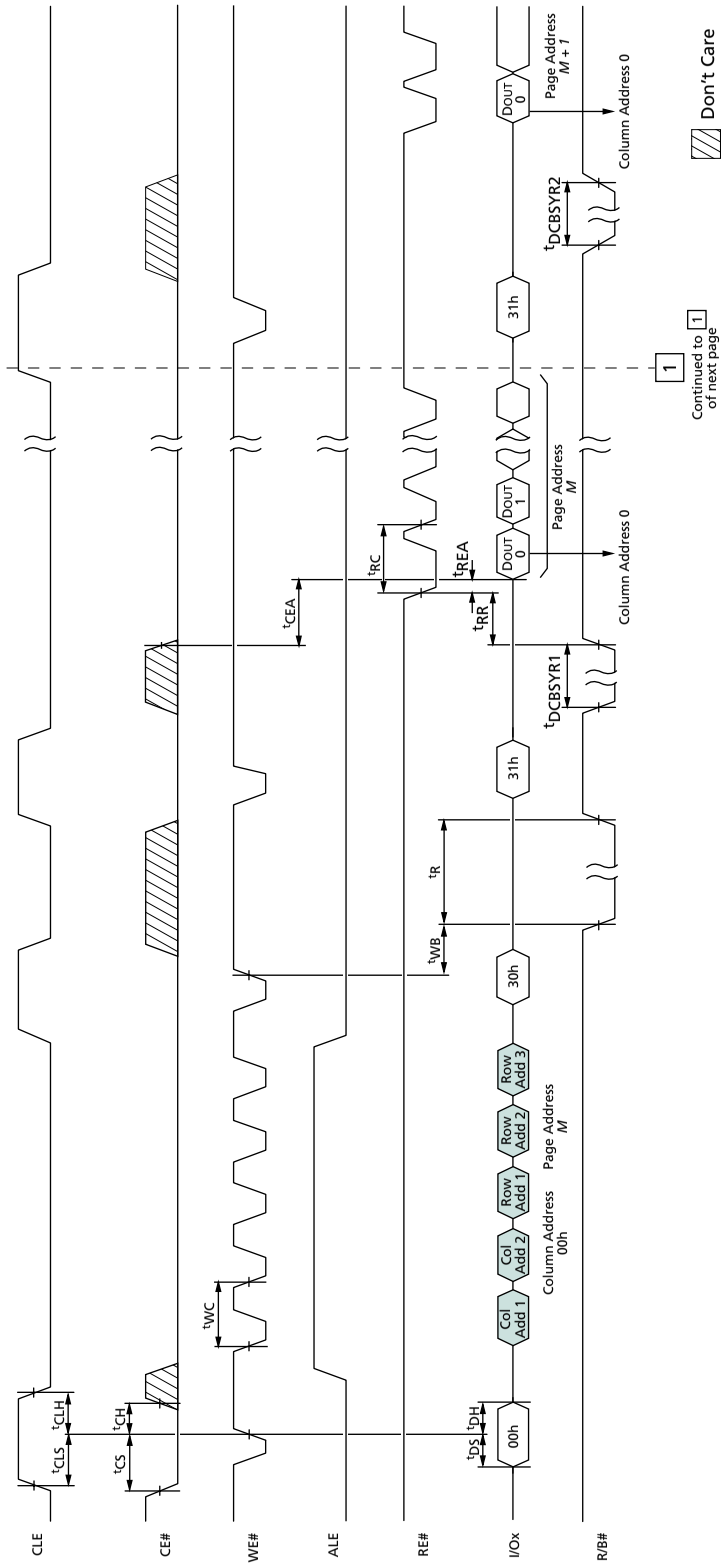


Figure 42: PAGE READ CACHE MODE Timing Diagram, Part 1 of 2

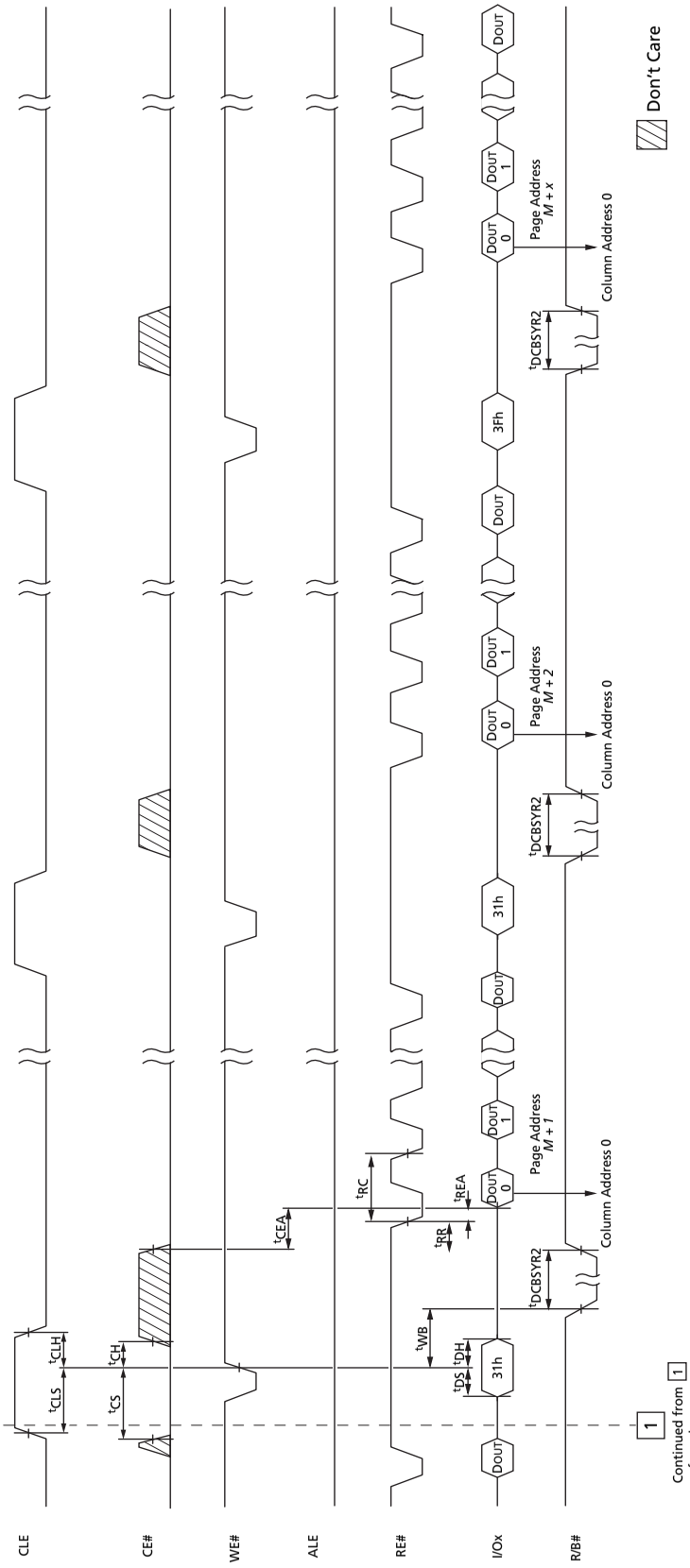


Figure 43: PAGE READ CACHE MODE Timing Diagram, Part 2 of 2

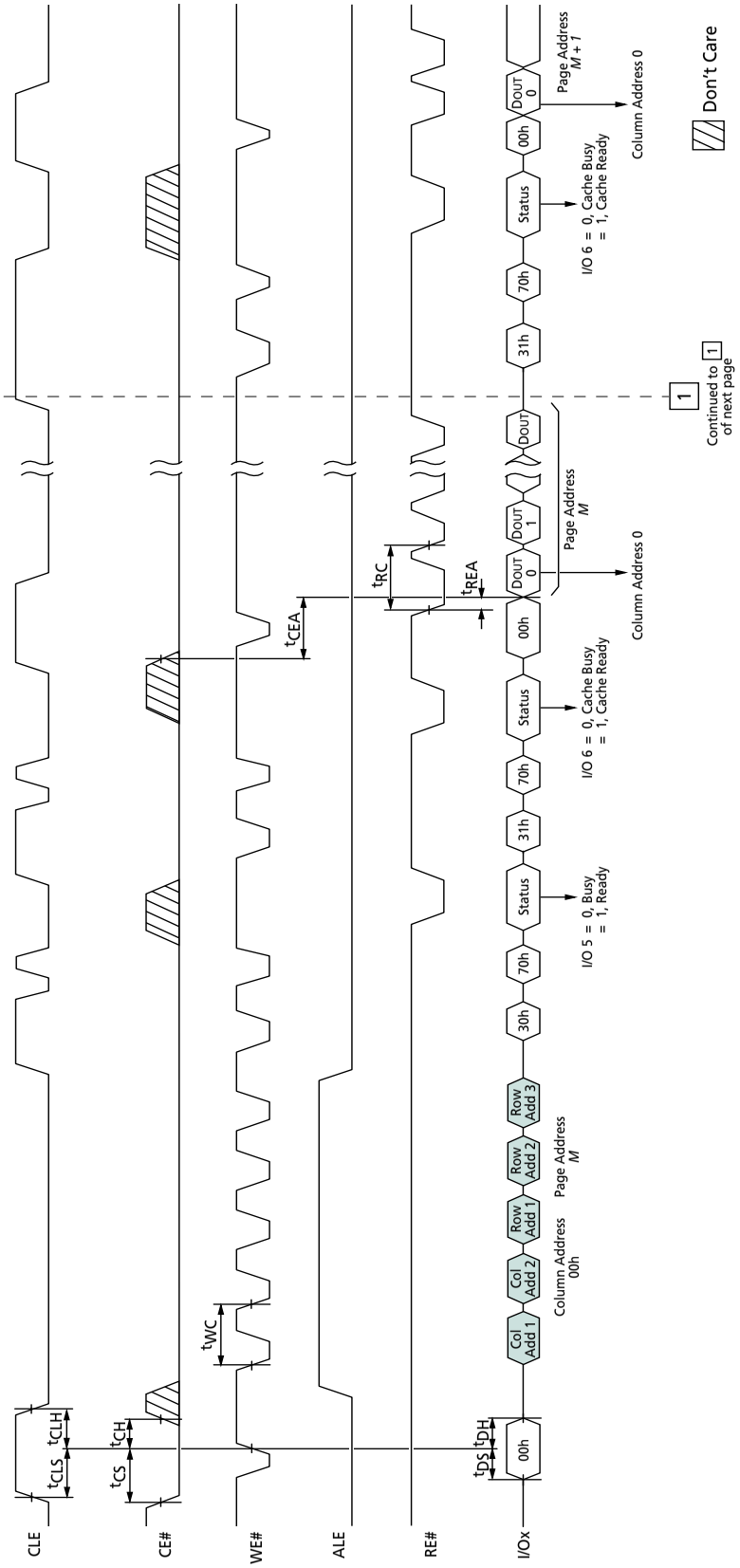


Figure 44: PAGE READ CACHE MODE Timing without R/B#, Part 1 of 2

Figure 45: PAGE READ CACHE MODE Timing without R/B#, Part 2 of 2

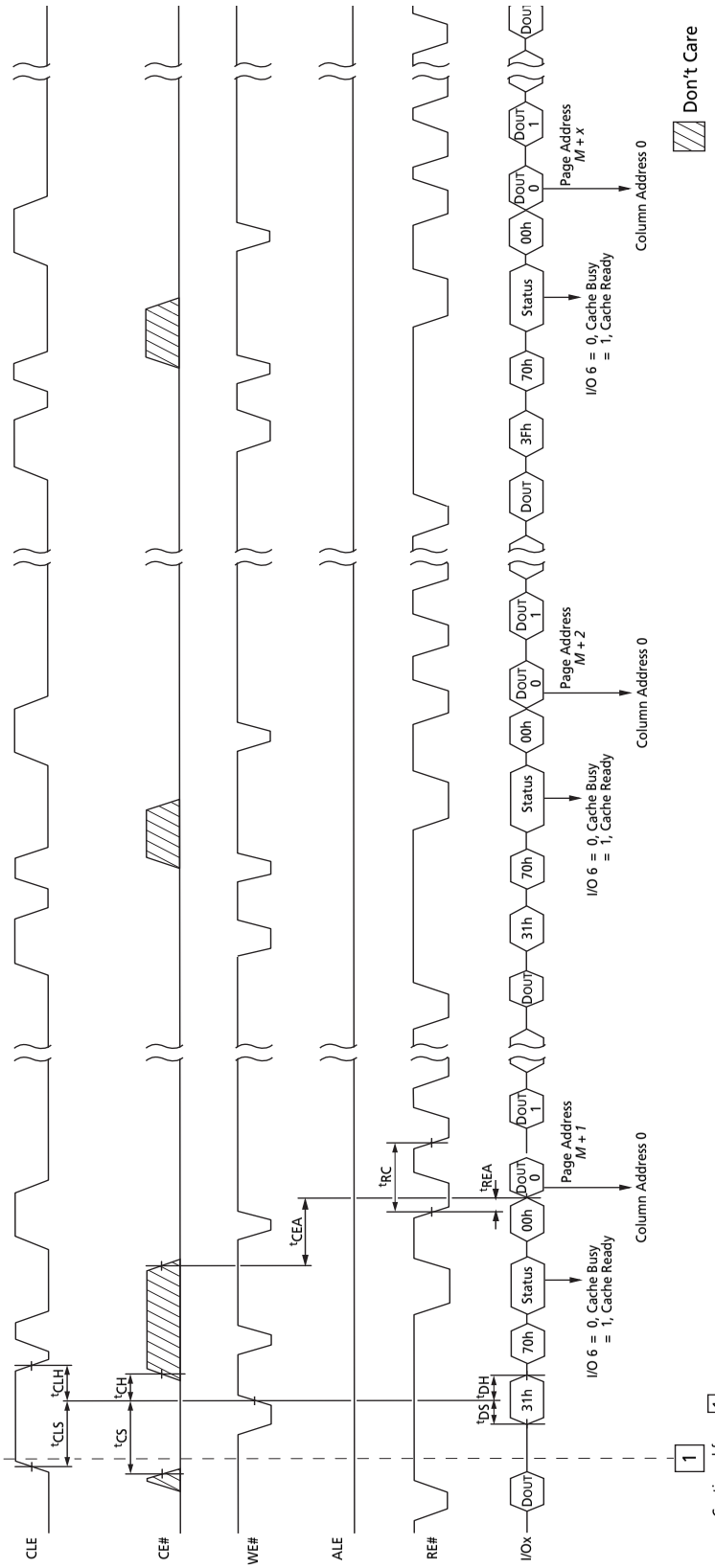


Figure 46: READ ID Operation

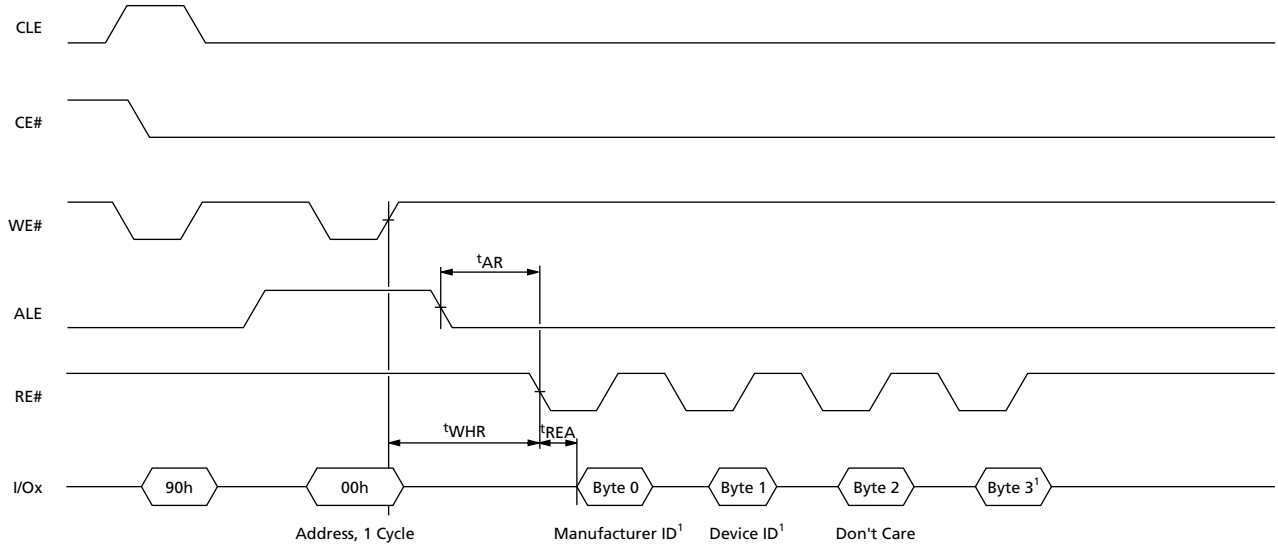


Figure 47: Program Operation with CE# "Don't Care"

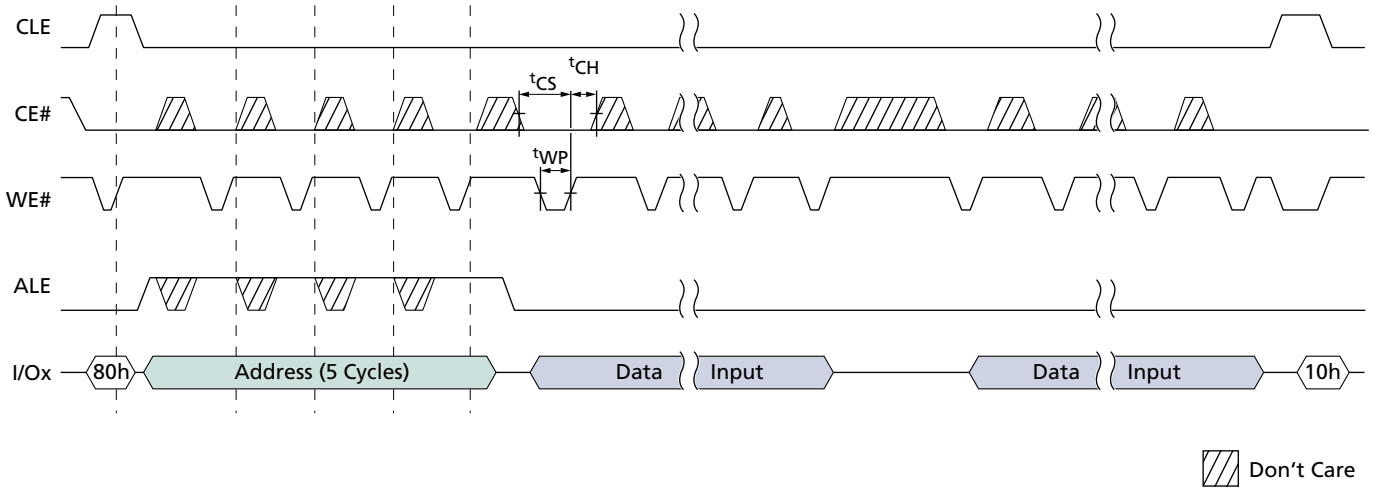


Figure 48: PROGRAM PAGE Operation

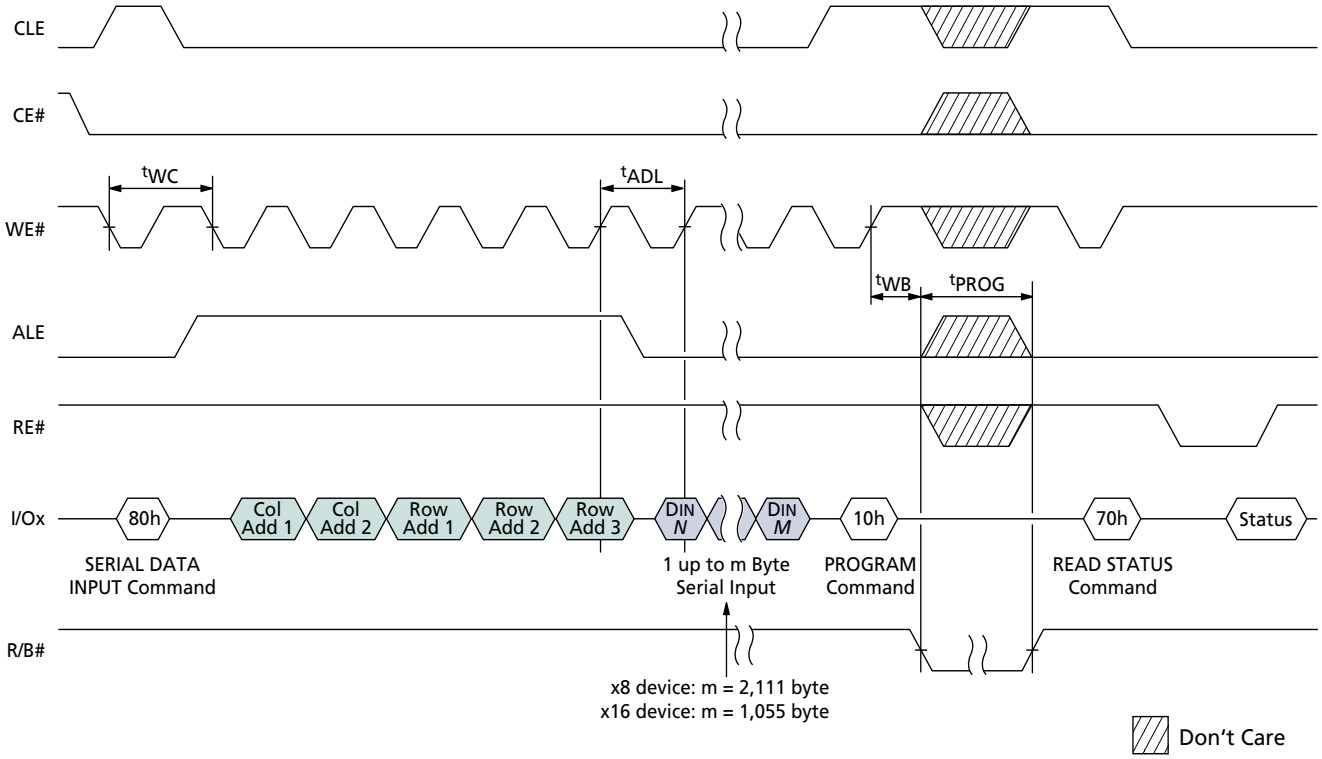


Figure 49: PROGRAM PAGE Operation with RANDOM DATA INPUT

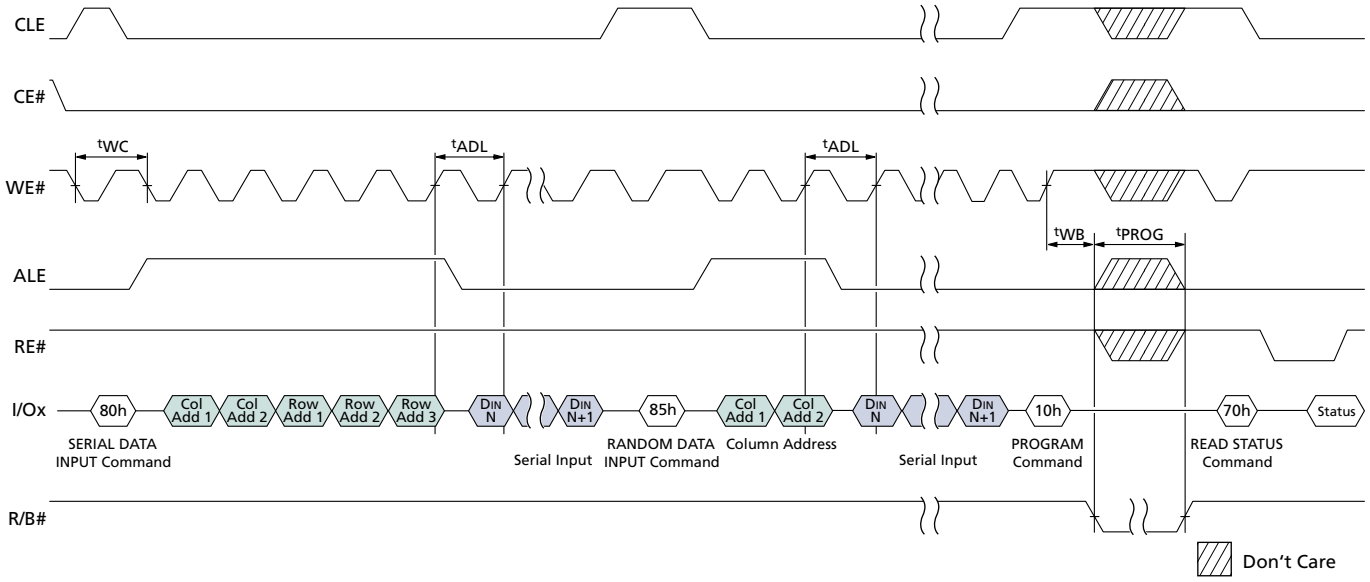


Figure 50: INTERNAL DATA MOVE

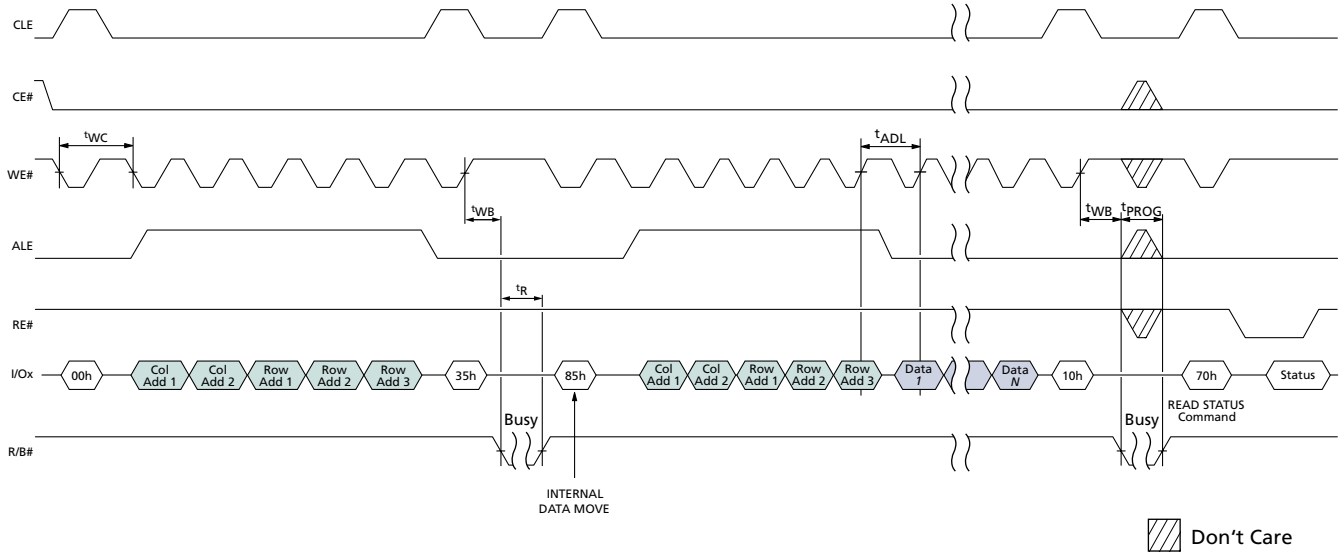
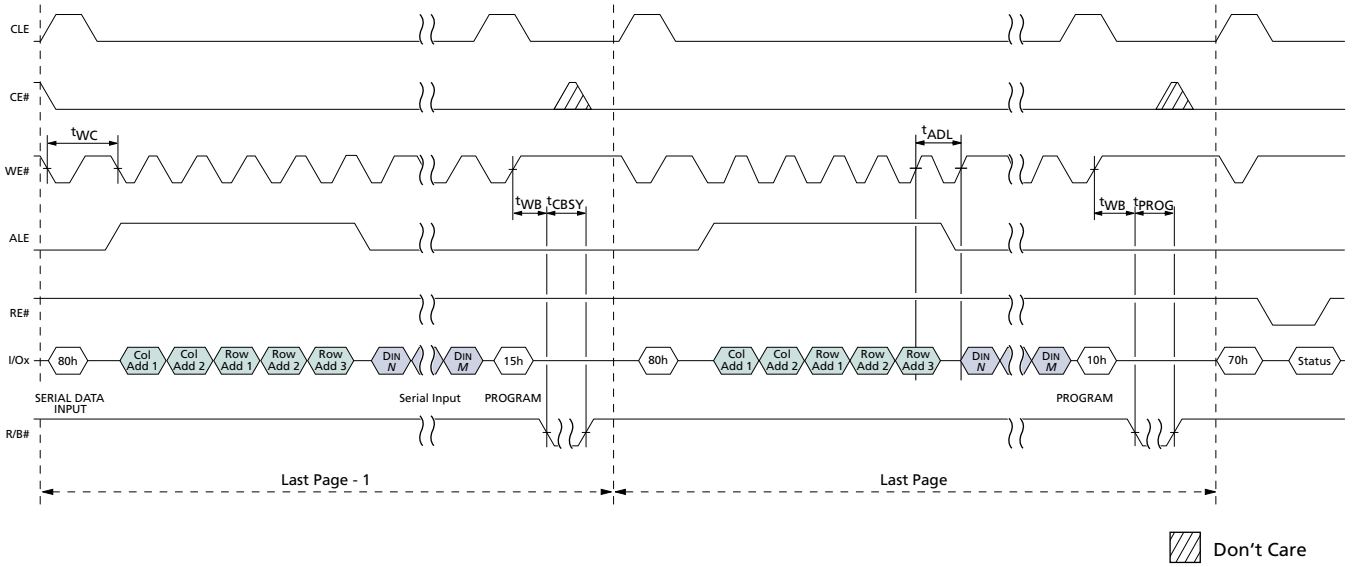


Figure 51: PROGRAM PAGE CACHE MODE



Note: PROGRAM PAGE CACHE MODE operations must not cross die address boundaries.

Figure 52: PROGRAM PAGE CACHE MODE Ending on 15h

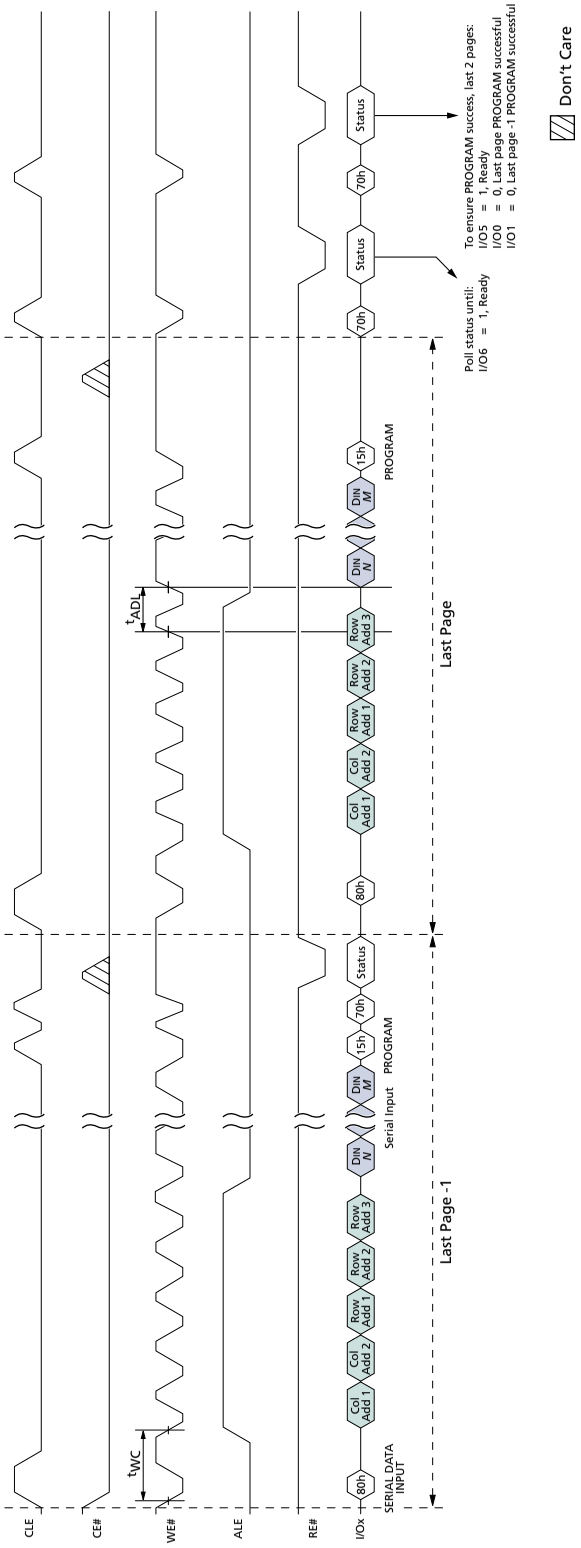
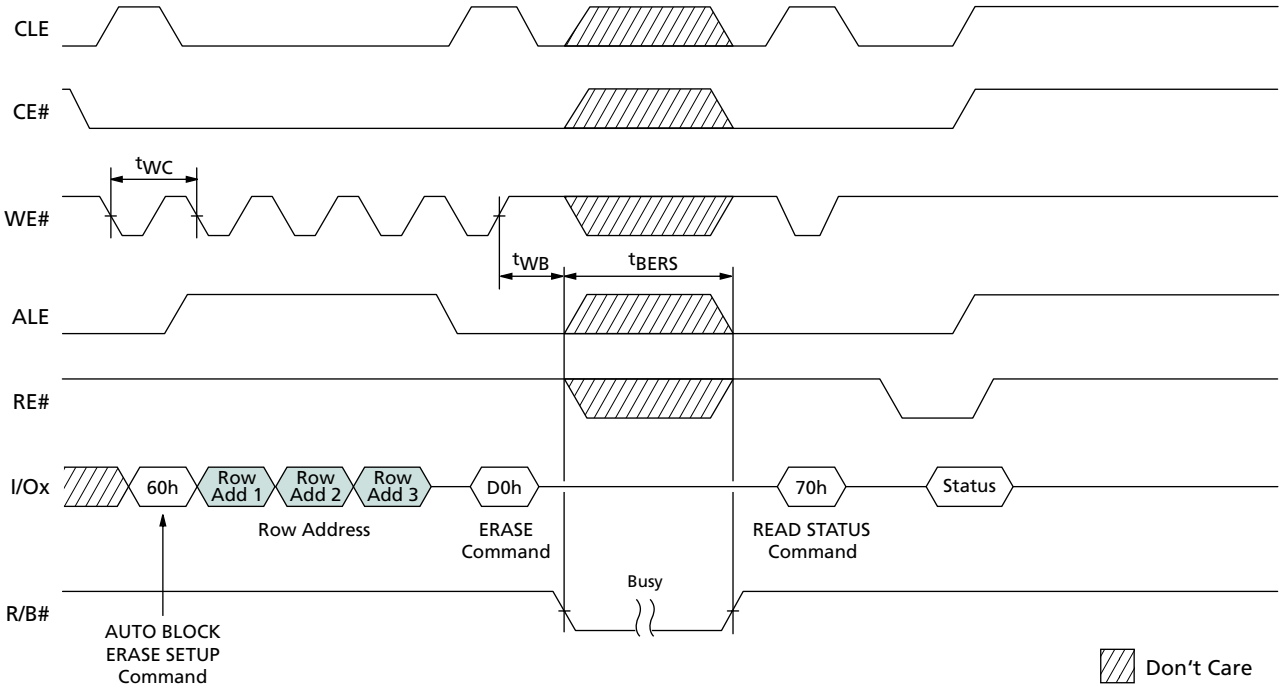
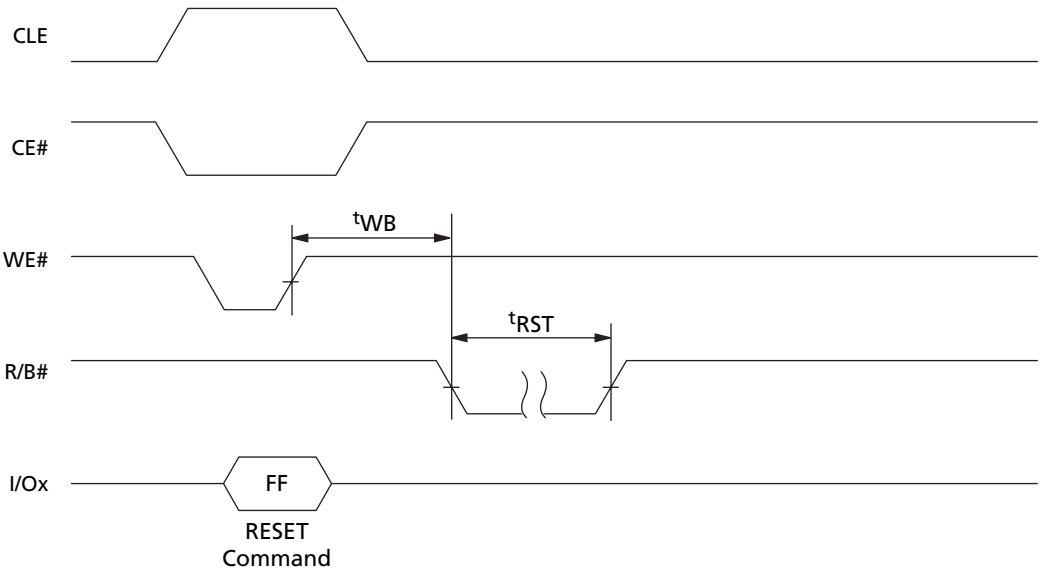


Figure 53: BLOCK ERASE Operation



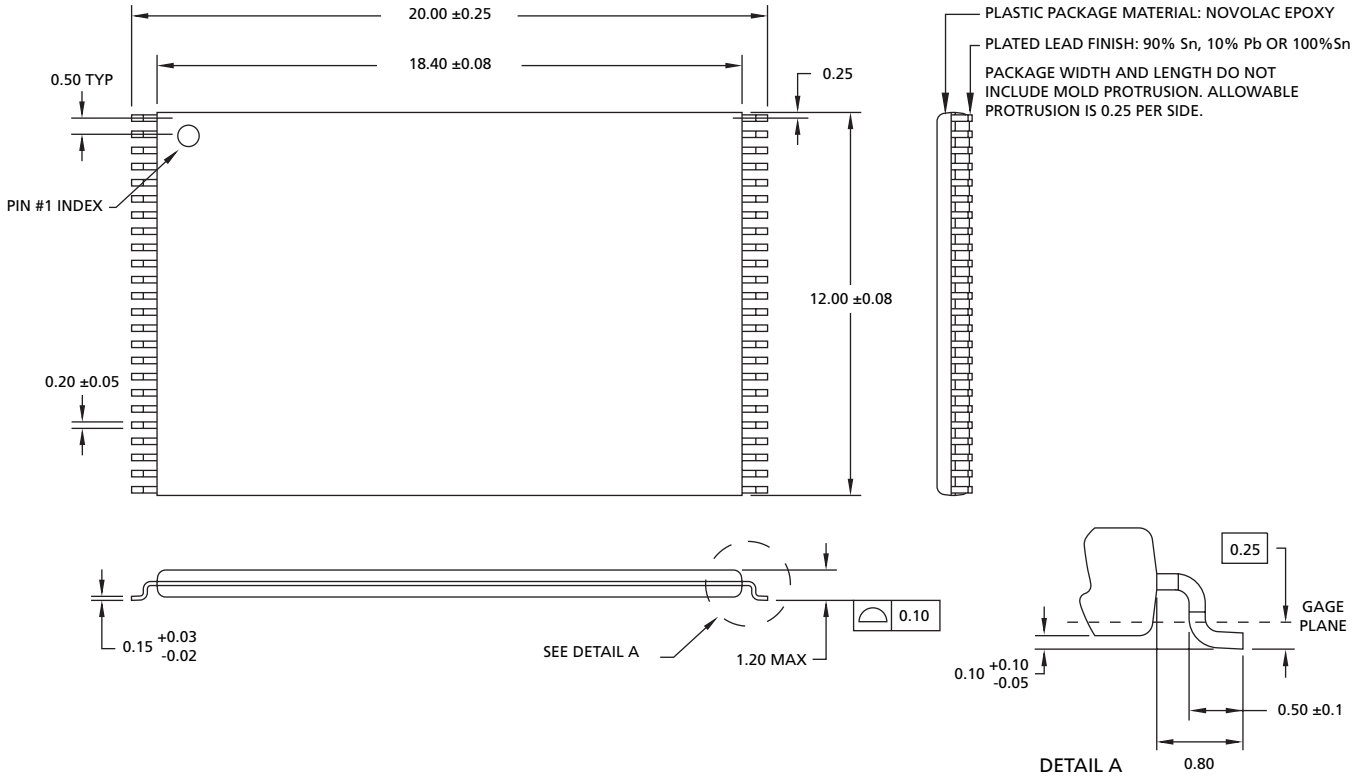
Notes: 1. See Table 8 on page 27 for actual values.

Figure 54: RESET Operation



Package Dimensions

Figure 55: 48-Pin TSOP Type I



Notes: 1. All dimensions in millimeters; MIN/MAX, or typical, as noted.
2. For design guidelines using the 8Gb device, see Micron technical note TN-29-09, at: www.micron.com/products/nand/massstorage/technote.

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Revision History

Rev. I 1/06
- "Options" on page 1 and Figure 2 on page 2: Added new 8Gb-only version of the lead-free 48-pin TSOP.
- "Error Management" on page 37: Clarified addressing and bad block marking description.
- "V_{CC} Power Cycling" on page 38: corrected to 2.0V for PROGRAM and ERASE operation disable.

Rev. H 9/05
- Updated READ STATUS 70h description.

Rev. G 9/05
- Clarified READ STATUS 70h description on page 27.
- Updated Figure 22 on page 28 and moved up under new description.

Rev. F 8/05
- Revised endurance feature on page 1: deleted "with ECC and invalid block mapping."
- Updated ^{t}R functional description.
- Added data retention period.
- Clarified AC characteristics.

Rev. E 7/05
- Replaced DNU definition in Table 1 on page 9.

Rev. D 6/05
- Updated address latch diagram.

Rev. C 5/05
- Added WRITE PROTECT.
- Updated standby current descriptions.

Rev. B 4/05
- Updated package drawing.

Rev. A 4/05
- Initial Release

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MT29F2G08ABAEAWP-AITX:E TR MT29F2G08ABAEAWP-ITX:E TR MT29F4G08ABAFAH4-AAT:F TR MT29F8G01ADAFD12-IT:F TR MT29F8G08ADAFAWP-AIT:F TR MT29F8G01ADBFD12-AAT:F TR MT29F8G01ADBFD12-IT:F TR MT29F8G08ADAFAH4-AAT:F TR MT29F4G01ABBFD12-AAT:F TR MT29F4G01ABBFD12-IT:F TR MT29F8G08ADAFAWP-AAT:F MT29F4G01ABBFDWB-IT:F MT29F4G01ABAFD12-AAT:F TR MT29F4G08ABAFAH4-AIT:F TR MT29F4G08ABBFAH4-AAT:F TR MT29F8G01ADAFD12-AAT:F TR MT29F2G01ABAGDWB-IT:G MT29F4G01ABAFDWB-IT:F MT29F4G08ABBFAH4-IT:F MT29F4G08ABAFAH4-IT:F MT29F4G08ABAFAWP-IT:F MT29F8G01ADAFD12-AAT:F MT29F4G08ABADAH4-AATX:D MT29F4G08ABADAWP-AATX:D MT29F4G08ABBEAH4-IT:E MT29F8G08ABBCAH4-IT:C MT29F8G08ADBDAH4-AAT:D MT29F2G08ABAGAWP-IT:G MT29F8G08ABACAH4-ITS:C TR MT29F8G16ADBDAH4-AIT:D TR MT29F2G01ABAGD12-AAT:G TR MT29F2G08ABAGAH4-IT:G MT29F2G08ABAGAWP-ITE:G MT29F2G08ABBGAH4-IT:G MT29F2G16ABBEAHC-AIT:E TR MT29F4G08ABBDAH4-AITX:D TR MT29F4G08ABBDAHC-AIT:D TR MT29F2G08ABAGAH4-IT:G TR MT29F2G08ABAGAH4-ITE:G TR MT29F2G08ABAGAWP-IT:G TR MT29F2G08ABAGAWP-ITE:G TR MT29F2G08ABBGAH4-IT:G TR MT29F2G16ABAEAWP-AIT:E TR MT29F2G01ABAGD12-IT:G TR MT29F2G01ABAGDSF-IT:G TR MT29F2G01ABAGDWB-IT:G TR MT29F2G01ABBGDWB-IT:G TR MT29F8G08ABBCAH4-IT:C TR MT29F8G16ABACAWP-IT:C TR MT29F2G08ABAEAH4-ITX:E TR MT29F2G08ABAEAH4-AITX:E TR MT29F8G08ABABAWP-AITX:B TR MT29F8G08ABABAWP-ITX:B TR MT29F8G08ABACAH4:C TR MT29F8G08ABACAH4-IT:C TR MT29F8G08ABBCAH4:C TR MT29F4G08ABBDAH4-ITX:D TR MT29F4G08ABBEAH4:E TR MT29F8G08ABABAWP:B TR MT29F4G08ABAEAH4:E TR MT29F4G08ABAEAH4-ITS:E TR MT29F4G08ABAEAWP:E TR MT29F4G08ABAEAWP-IT:E TR MT29F2G08ABBEAH4-ITX:E TR MT29F4G08ABADAH4-ITX:D TR